

# EE 330

## Lecture 16

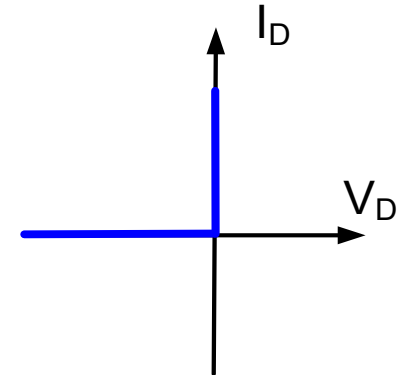
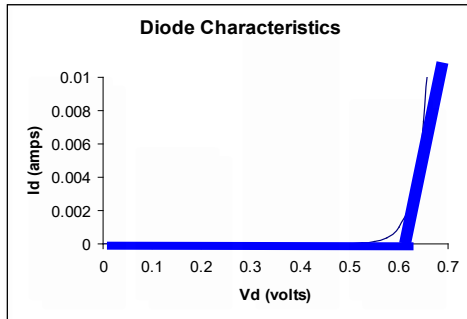
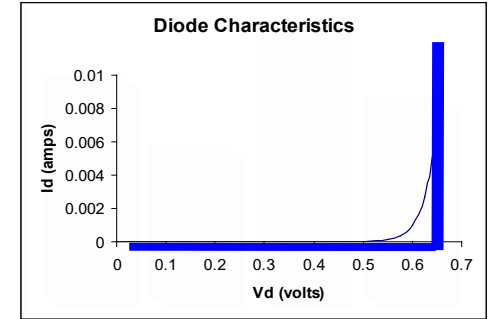
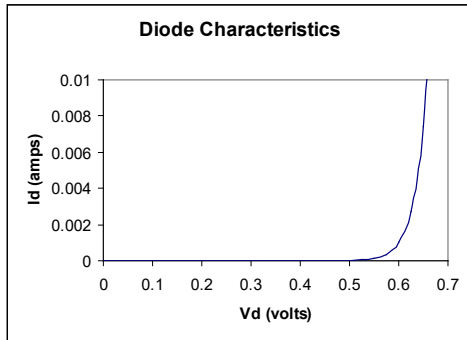
### Devices in Semiconductor Processes

- Diodes (continued)
- Capacitors
- MOSFETs

# Fall 2023 Exam Schedule

Exam 1	Friday Sept 22	
Exam 2	Friday Oct 20	
Exam 3	Friday Nov. 17	
Final	Monday Dec 11	12:00 – 2:00 p.m.

# Diode Models



Which model should be used?

The simplest model that will give acceptable results in the analysis of a circuit

# Use of Piecewise Models for Nonlinear Devices when Analyzing Electronic Circuits

Process:

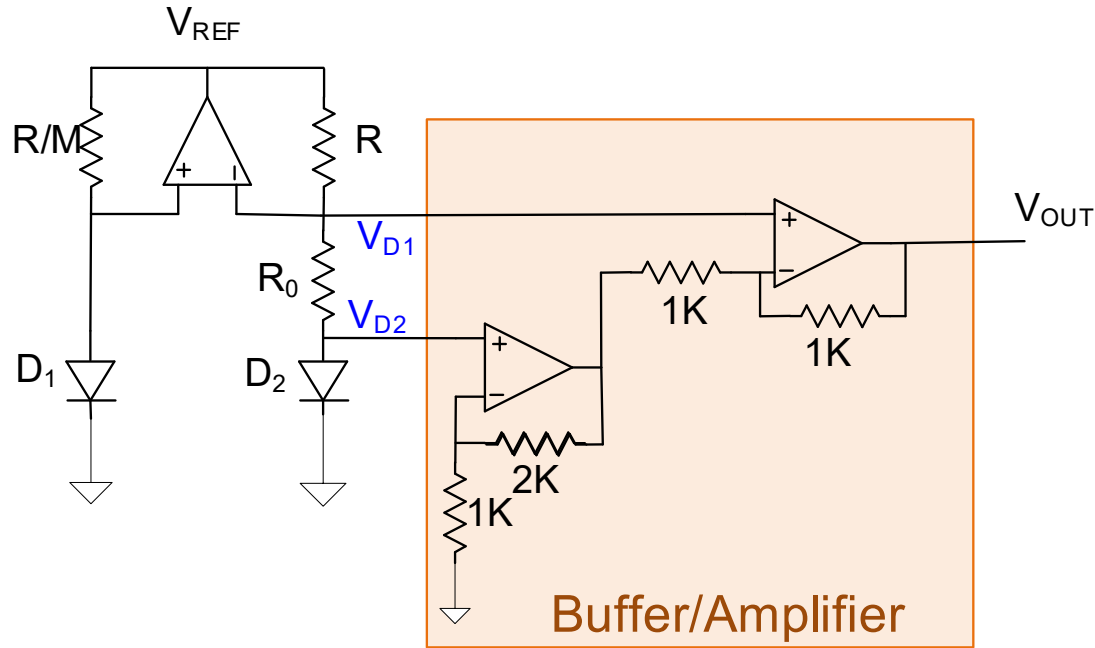
1. Guess state of the device
2. Analyze circuit
3. Verify State
4. Repeat steps 1 to 3 if verification fails
5. Verify model (if necessary)

Observations:

- Analysis generally simplified dramatically (particularly if piecewise model is linear)
- Approach applicable to wide variety of nonlinear devices
- Closed-form solutions give insight into performance of circuit
- Usually much faster than solving the nonlinear circuit directly
- Wrong guesses in the state of the device do not compromise solution (verification will fail)
- Helps to guess right the first time
- Detailed model is often not necessary with most nonlinear devices
- Particularly useful if piecewise model is PWL (but not necessary)
- For practical circuits, the simplified approach usually applies

**Key Concept For Analyzing Circuits with Nonlinear Devices**

# A Diode Application



If buffer/amplifier added, serves as temperature sensor at  $V_{OUT}$

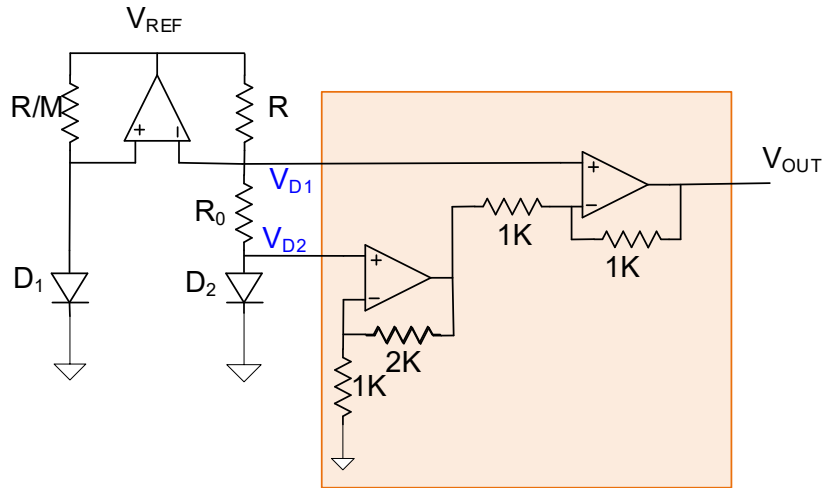
$$V_{OUT} = 2(V_{D1} - V_{D2})$$

May need compensation and startup circuits

For appropriate  $R_0$ , serves as bandgap voltage reference (buffer/amplifier excluded)

$$V_{REF} = V_{D1} + \frac{R}{R_0}(V_{D1} - V_{D2})$$

# A Diode Application



$$V_{OUT} = 2(V_{D1} - V_{D2})$$

Analysis of temperature sensor (assume  $D_1$  and  $D_2$  matched)

$$I_{D2}(T) = \left( J_{SX} \left[ T^m e^{\frac{-V_{G0}}{V_t}} \right] \right) A e^{\frac{V_{D2}}{V_t}}$$

$$I_{D1}(T) = \left( J_{SX} \left[ T^m e^{\frac{-V_{G0}}{V_t}} \right] \right) A e^{\frac{V_{D1}}{V_t}}$$

$$I_{D1}(T) = M I_{D2}(T)$$

$$V_t = \frac{k}{q} T$$

$$\left( J_{SX} \left[ T^m e^{\frac{-V_{G0}}{V_t}} \right] \right) A e^{\frac{V_{D1}}{V_t}} = M \left( J_{SX} \left[ T^m e^{\frac{-V_{G0}}{V_t}} \right] \right) A e^{\frac{V_{D2}}{V_t}}$$

Cancelling terms and taking ln we obtain

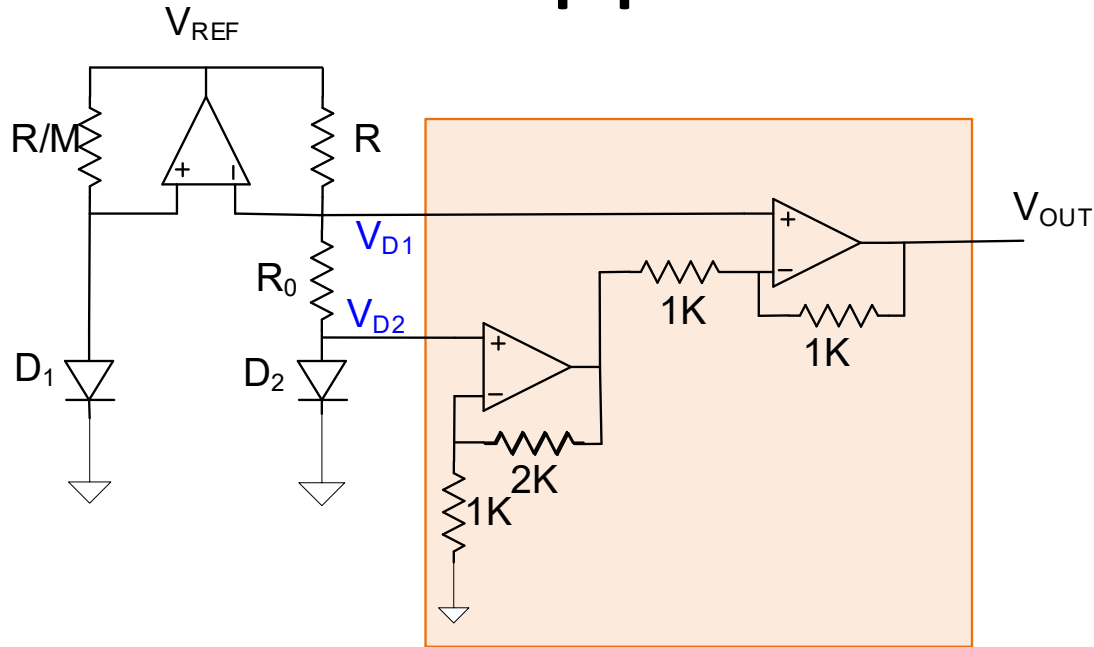
$$V_{D1} - V_{D2} = V_t \ln M$$

Thus

$$V_{OUT} = 2(V_{D1} - V_{D2}) = 2 \ln M \cdot \frac{k}{q} T$$

$$T = V_{OUT} \frac{q}{2k \ln M}$$

# A Diode Application



May need compensation and startup circuits

If buffer/amplifier added, serves as temperature sensor at  $V_{OUT}$

$$V_{OUT} = 2(V_{D1} - V_{D2}) \quad \longrightarrow \quad T = V_{OUT} \frac{q}{2k \ln M}$$

For appropriate  $R_0$ , serves as bandgap voltage reference

$$V_{REF} = V_{D1} + \frac{R}{R_0}(V_{D1} - V_{D2}) \quad \longrightarrow \quad ?$$

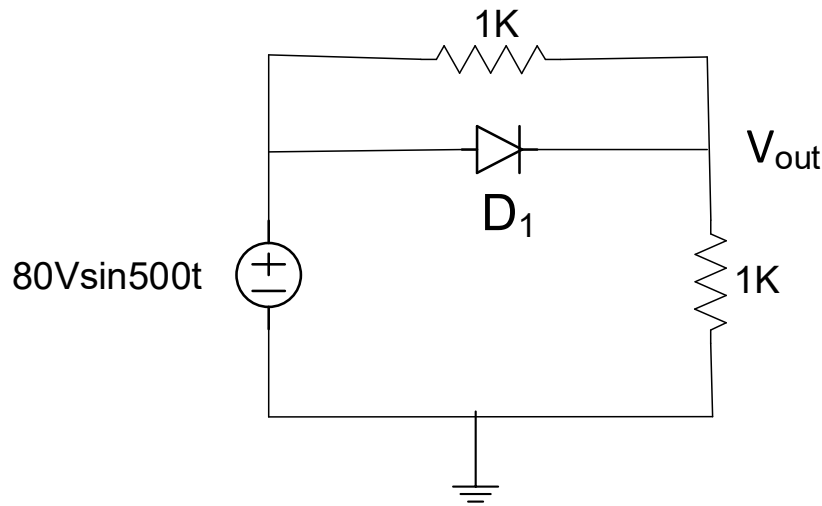
Analysis of  $V_{REF}$  to show output is nearly independent of  $T$  and  $V_{DD}$  is more tedious

# Use of Piecewise Models for Nonlinear Devices when Analyzing Electronic Circuits

Process:

1. Guess state of the device
2. Analyze circuit
3. Verify State
4. Repeat steps 1 to 3 if verification fails
5. Verify model (if necessary)

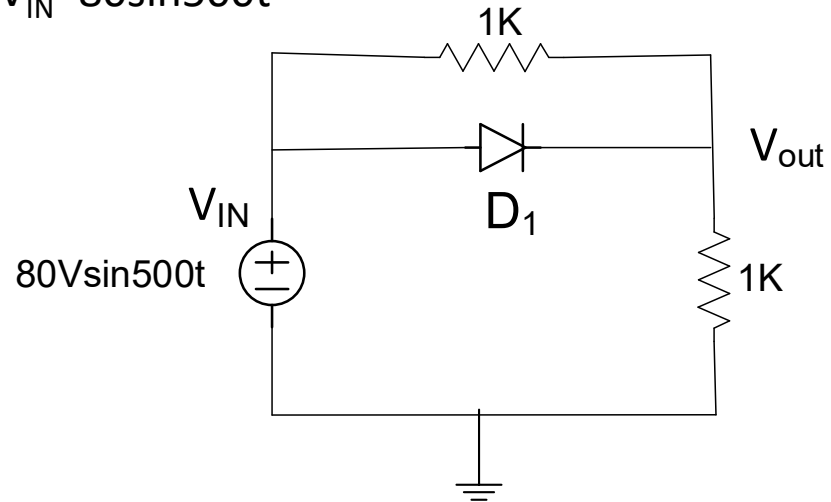
What about nonlinear circuits (using piecewise models) with time-varying inputs?



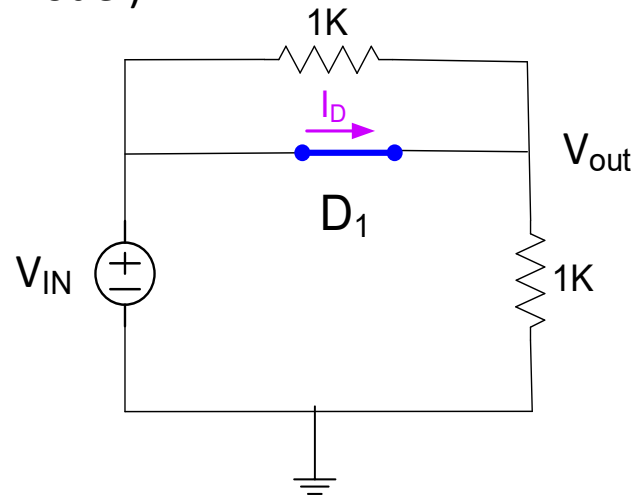
Same process except state verification (step 3) may include a range where solution is valid



Example: Determine  $V_{OUT}$  for  $V_{IN}=80\sin 500t$



Guess  $D_1$  ON (will use ideal diode model)

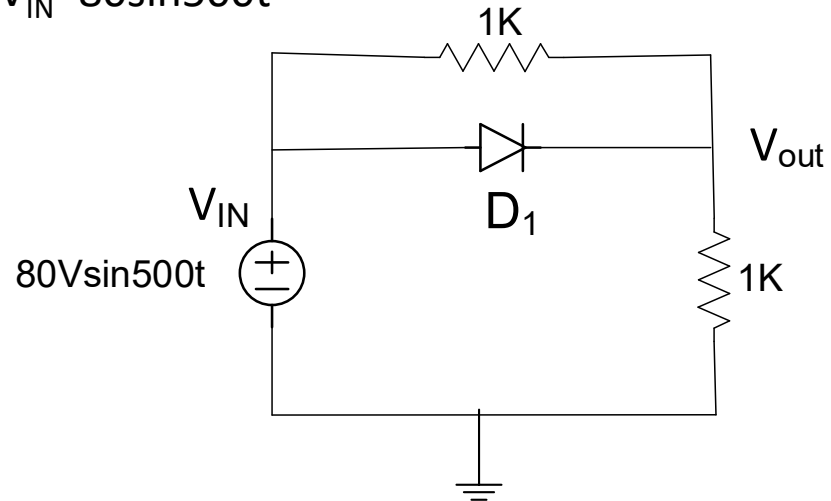


$$V_{OUT}=V_{IN}=80\sin(500t)$$

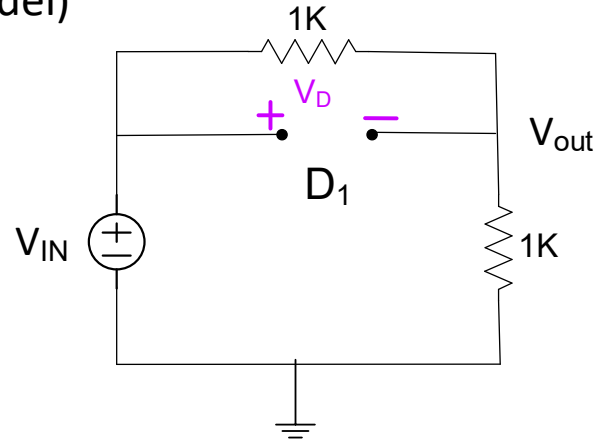
Valid for  $I_D > 0$        $I_D = \frac{V_{IN}}{1K}$

Thus valid for  $V_{IN} > 0$

Example: Determine  $V_{OUT}$  for  $V_{IN}=80\sin 500t$



Guess  $D_1$  OFF (will use ideal diode model)

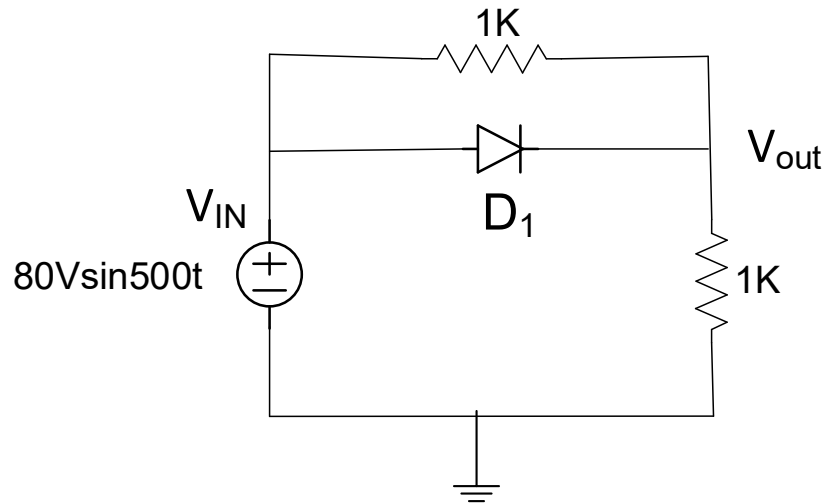


$$V_{OUT}=V_{IN}/2=40\sin(500t)$$

Valid for  $V_D < 0$       $V_D = \frac{V_{IN}}{2}$

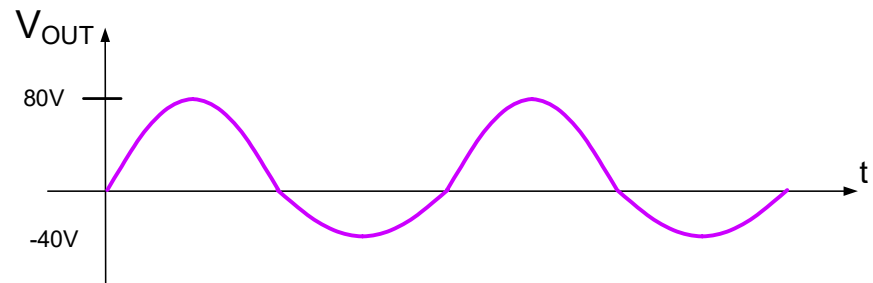
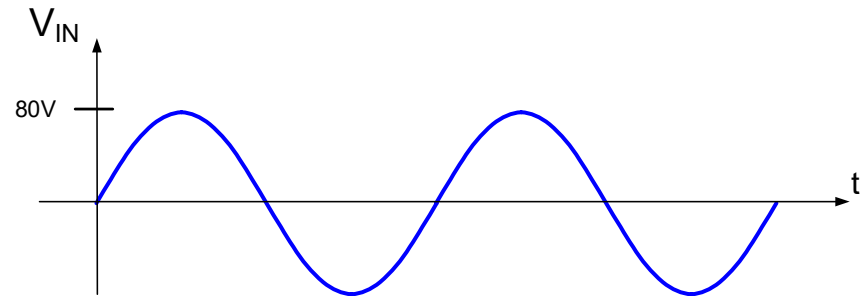
Thus valid for  $V_{IN} < 0$

Example: Determine  $V_{OUT}$  for  $V_{IN}=80\sin 500t$



Thus overall solution

$$V_{OUT} = \begin{cases} 80 \sin 500t & \text{for } V_{IN} > 0 \\ 40 \sin 500t & \text{for } V_{IN} < 0 \end{cases}$$

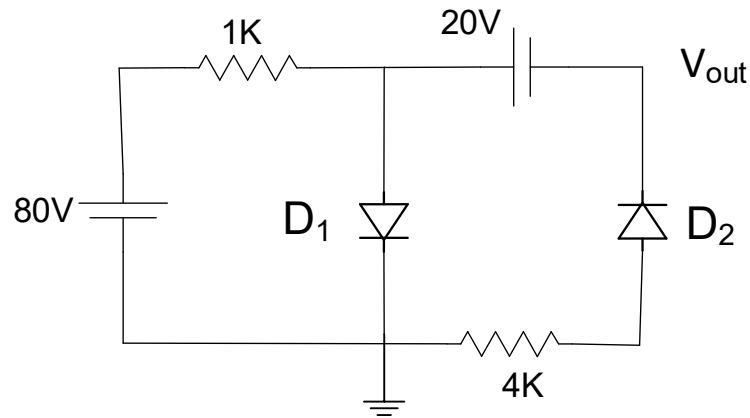


# Use of Piecewise Models for Nonlinear Devices when Analyzing Electronic Circuits

Process:

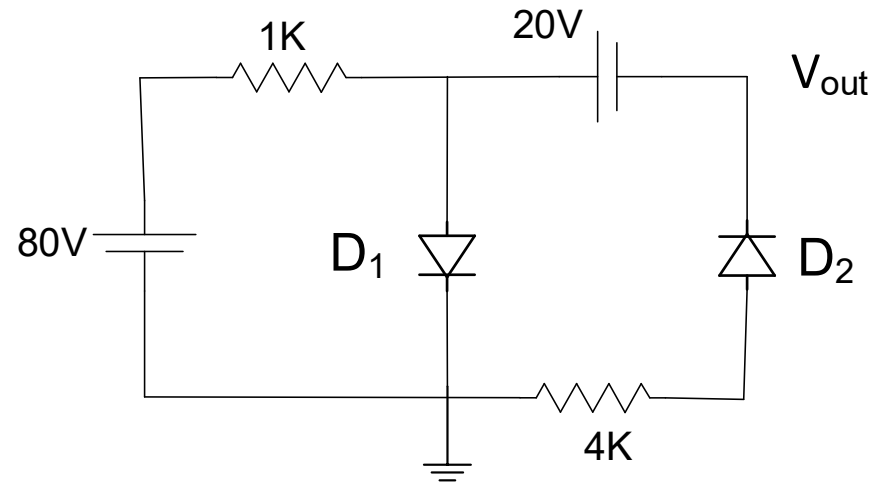
1. Guess state of the device
2. Analyze circuit
3. Verify State
4. Repeat steps 1 to 3 if verification fails
5. Verify model (if necessary)

What about circuits (using piecewise models) with multiple nonlinear devices?

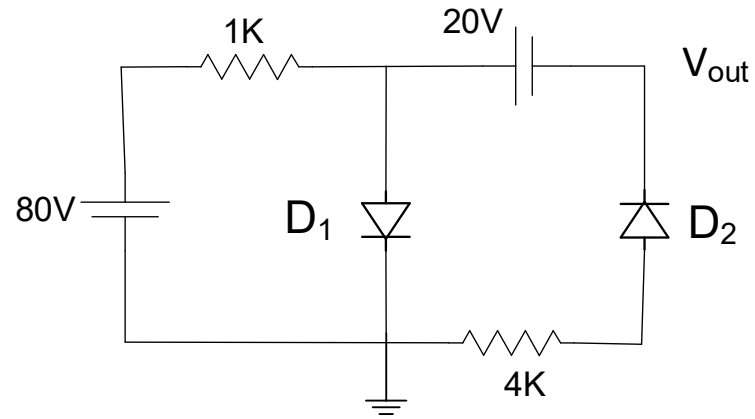


Guess state for each device (multiple combinations possible)

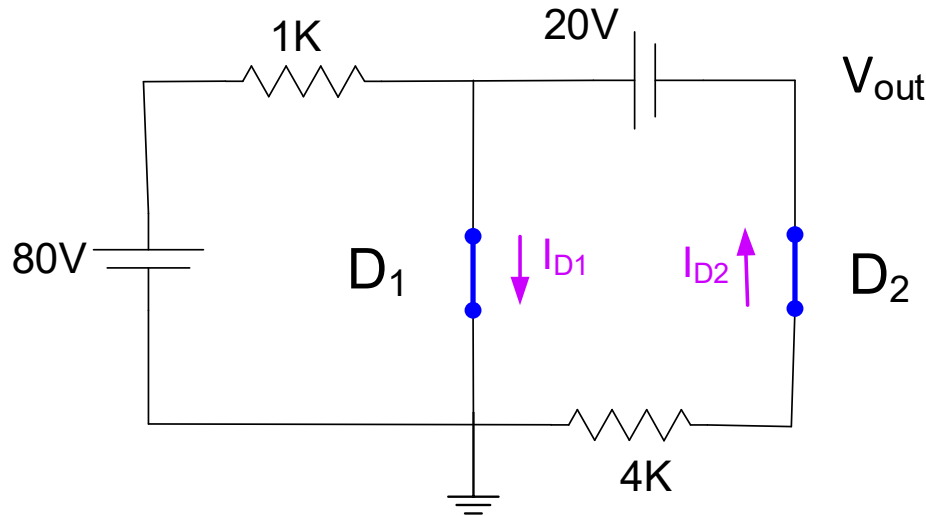
Example: Obtain  $V_{OUT}$



Example: Obtain  $V_{OUT}$



Guess  $D_1$  and  $D_2$  on



$$V_{OUT} = -20V$$

Valid for  $I_{D2} > 0$  and  $I_{D1} > 0$

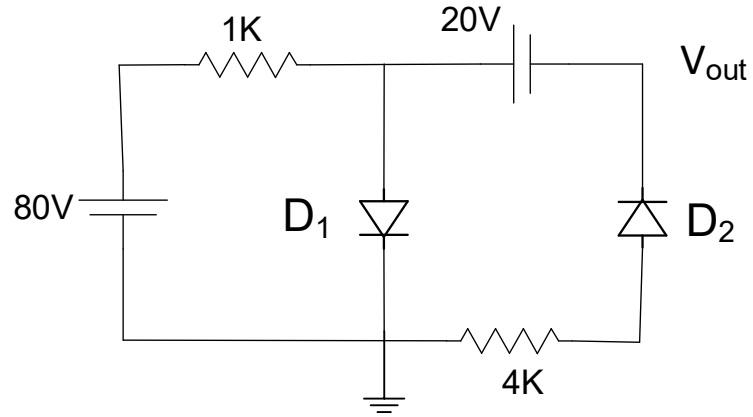
$$I_{D2} = \frac{20V}{4K} = 5mA > 0 \quad I_{D1} = \frac{80V}{1K} + I_{D2} = 85mA > 0$$

Validates

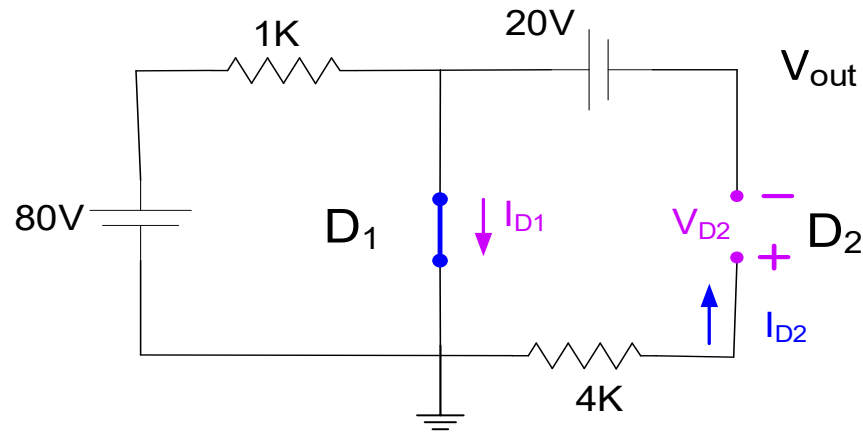
Validates

Since validates, solution is valid

Example: Obtain  $V_{OUT}$



If we had guessed wrong  
Guess  $D_1$  ON and  $D_2$  OFF



$$V_{OUT} = -20V$$

Valid for  $I_{D1} > 0$  and

$$V_{D2} < 0$$

$$I_{D1} = \frac{80V}{1K} + I_{D2} = 80mA > 0$$

$$V_{D2} = +20$$

Validates

FAILS  
Validation

Since fails to validate, solution is not valid so guess is wrong !

# Use of Piecewise Models for Nonlinear Devices when Analyzing Electronic Circuits

## Single Nonlinear Device

Process:

1. Guess state of the device
2. Analyze circuit
3. Verify State
4. Repeat steps 1 to 3 if verification fails
5. Verify model (if necessary)

## Multiple Nonlinear Devices

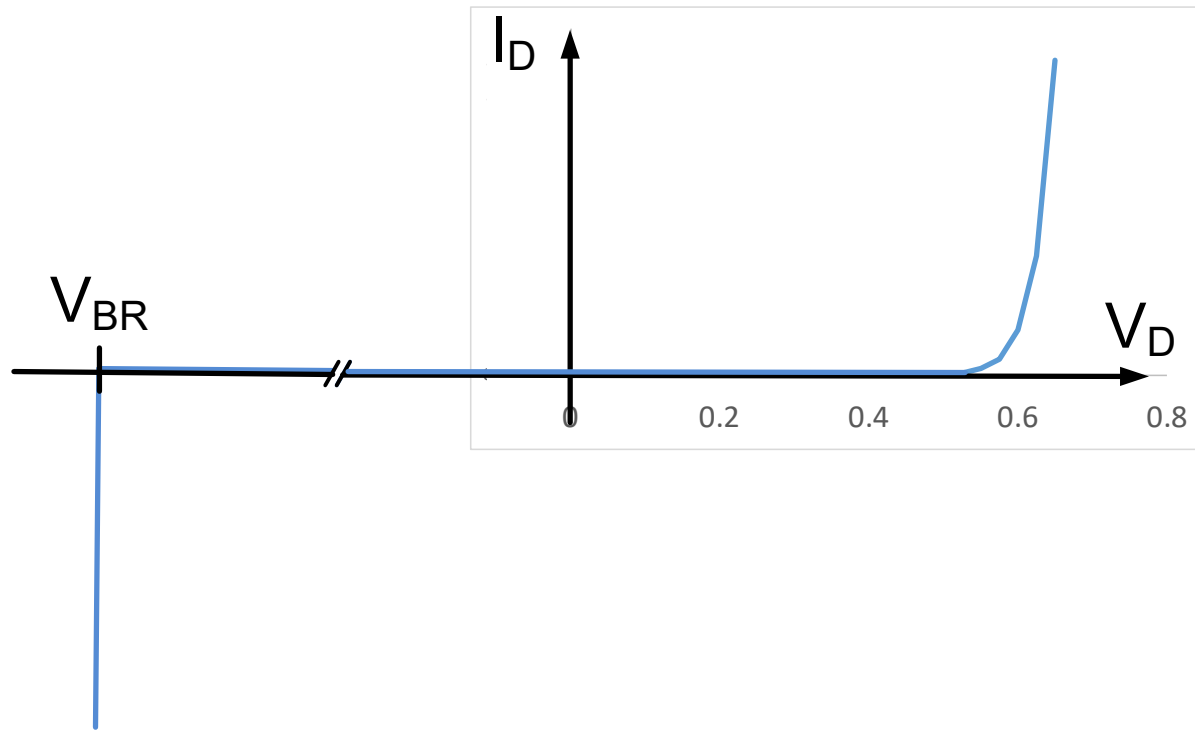
Process:

1. Guess state of each device (may be multiple combinations)
2. Analyze circuit
3. Verify State
4. Repeat steps 1 to 3 if verification fails
5. Verify models (if necessary)

Analytical solutions of circuits with multiple nonlinear devices are often impossible to obtain if detailed non-piecewise nonlinear models are used



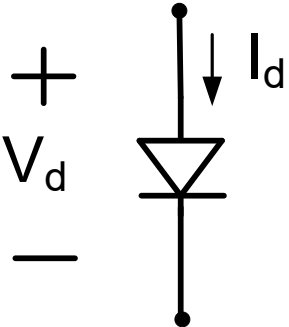
# Diode Breakdown



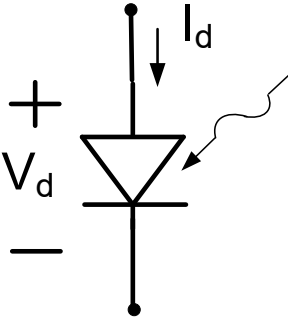
- Diodes will “break down” if a large reverse bias is applied
- Unless current is limited, reverse breakdown is destructive
- Breakdown is very sharp
- For many signal diodes,  $V_{BR}$  is in the -100V to -1000V range
- Relatively easy to design circuits so that with correct diodes, breakdown will not occur
- Zener diodes have a relatively small breakdown and current is intentionally limited to use this breakdown to build voltage references

# Types of Diodes

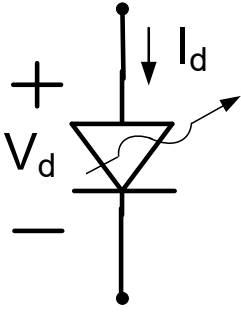
## pn junction diodes



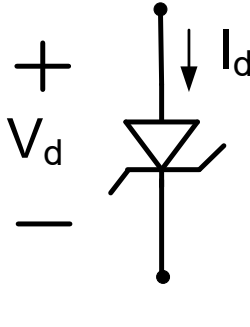
Signal or Rectifier



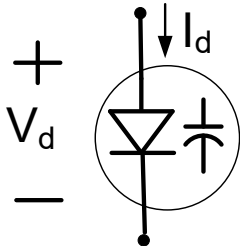
Pin or Photo



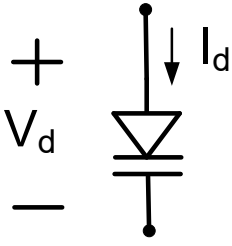
Light Emitting LED  
Laser Diode



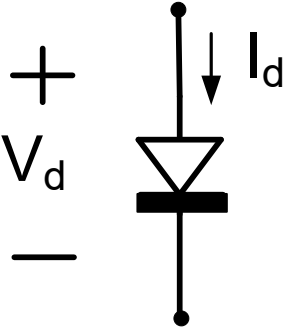
Zener



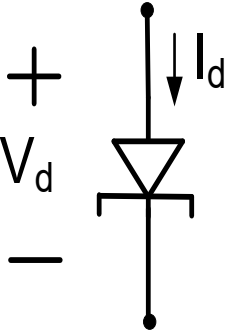
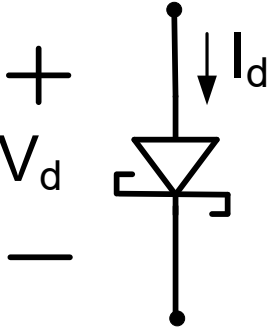
Varactor or Varicap



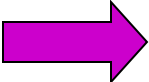
## Metal-semiconductor junction diodes



Schottky Barrier



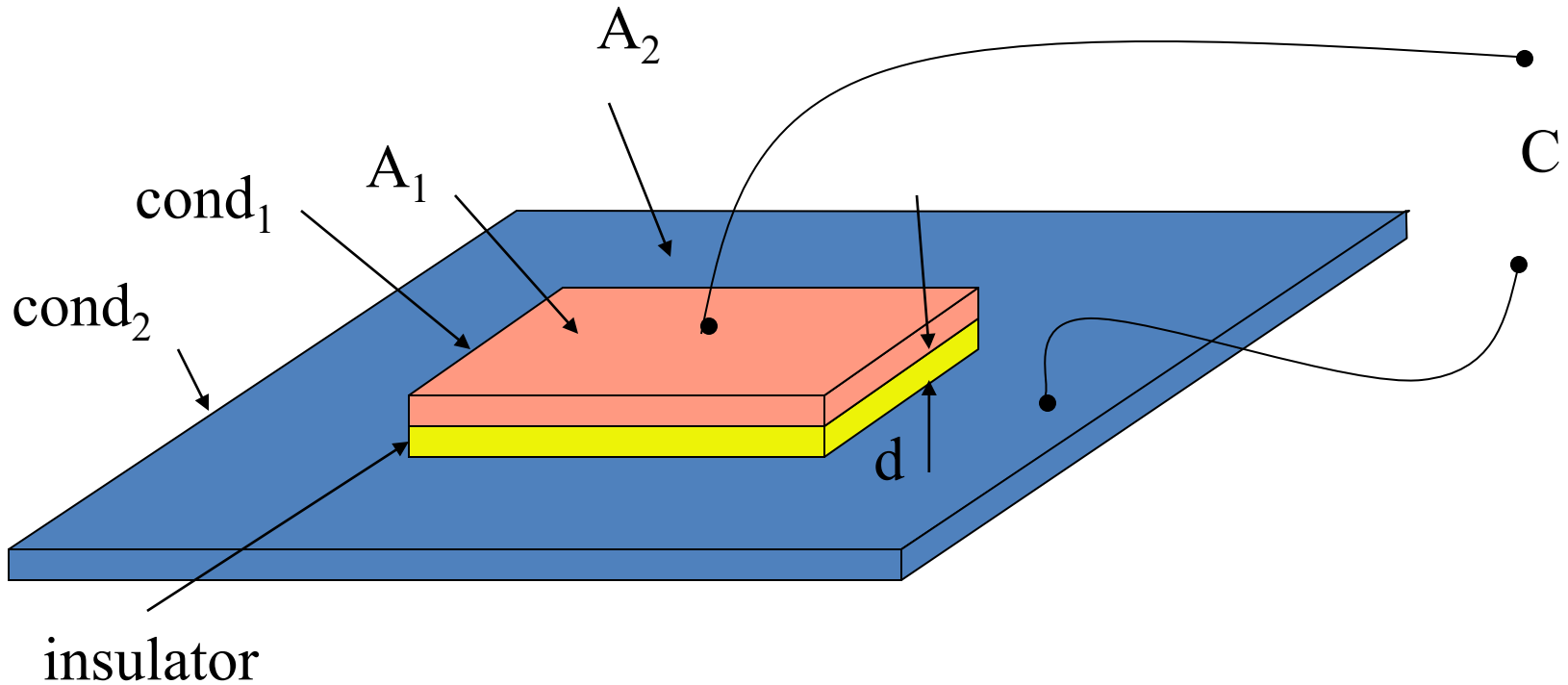
# Basic Devices and Device Models

- Resistor
- Diode
-  Capacitor
- MOSFET
- BJT

# Capacitors

- Types
  - Parallel Plate
  - Fringe
  - Junction

# Parallel Plate Capacitors



$A$  = area of intersection of  $A_1$  &  $A_2$

One (top) plate **intentionally** sized smaller to determine  $C$

$$C = \frac{\epsilon A}{d}$$

# Parallel Plate Capacitors

$$\text{If } C_d = \frac{\text{Cap}}{\text{unit area}}$$

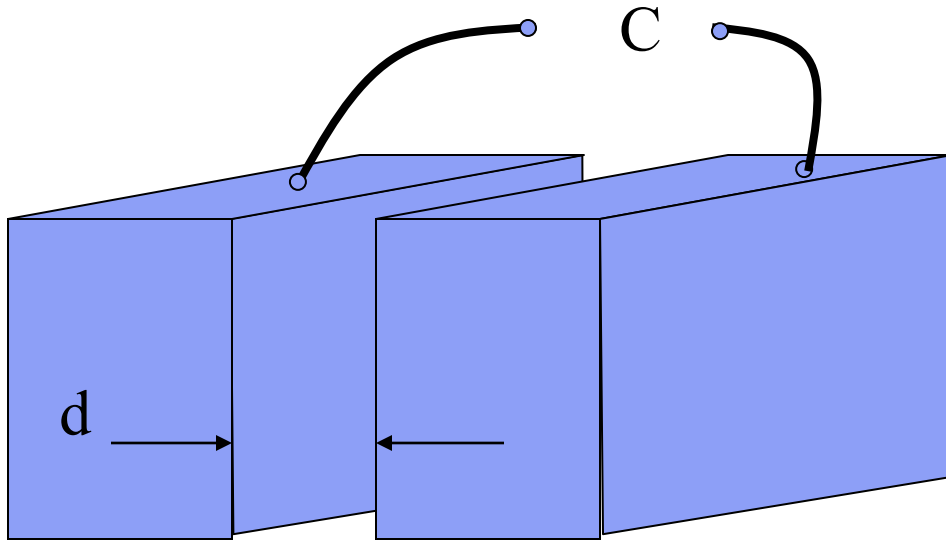
$$C = \frac{\epsilon A}{d}$$

$$C = C_d A$$

where

$$C_d = \frac{\epsilon}{d}$$

# Fringe Capacitors

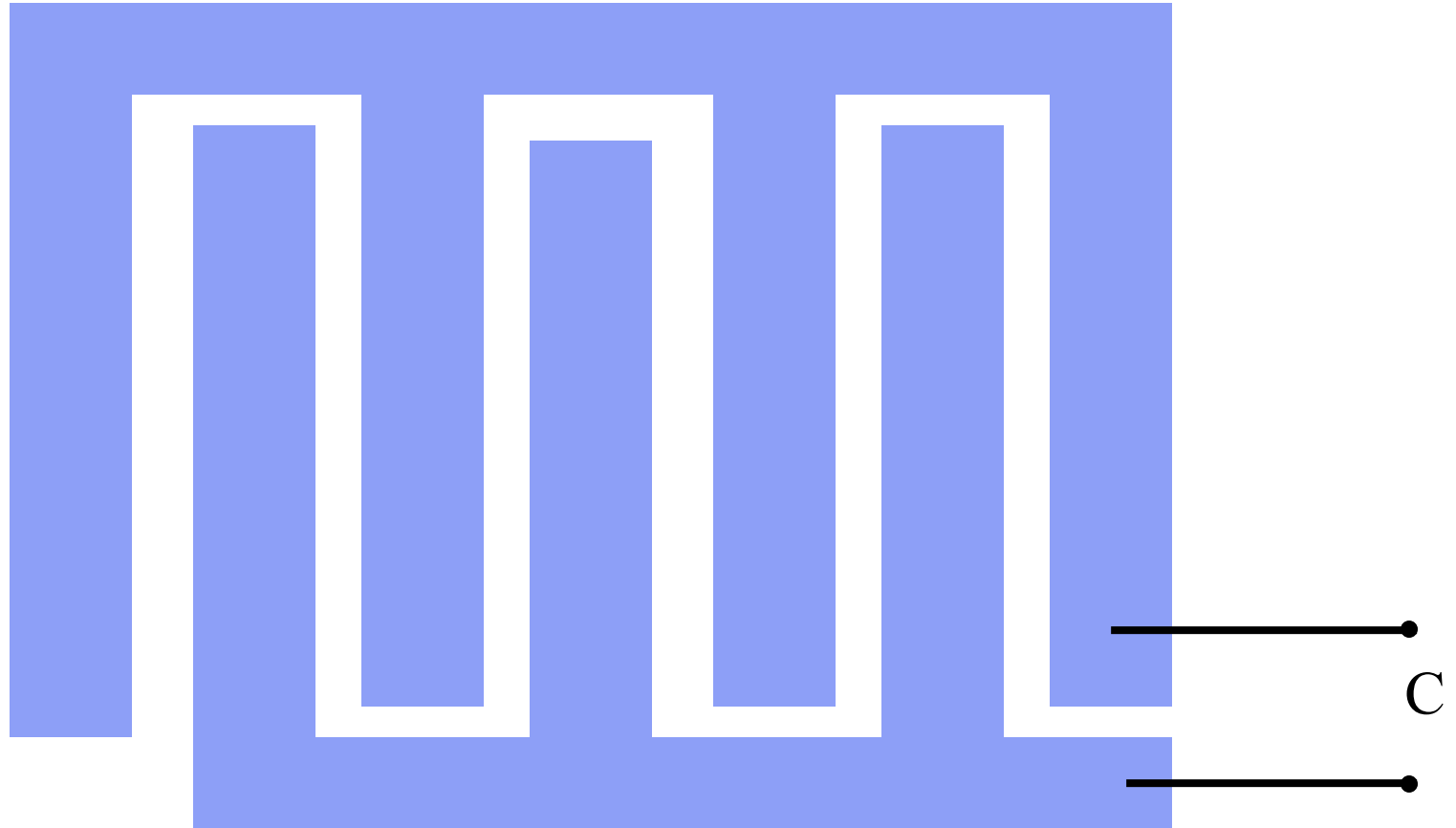


$$C = \frac{\epsilon A}{d}$$

A is the area where the two plates are parallel

Only a single layer is needed to make fringe capacitors

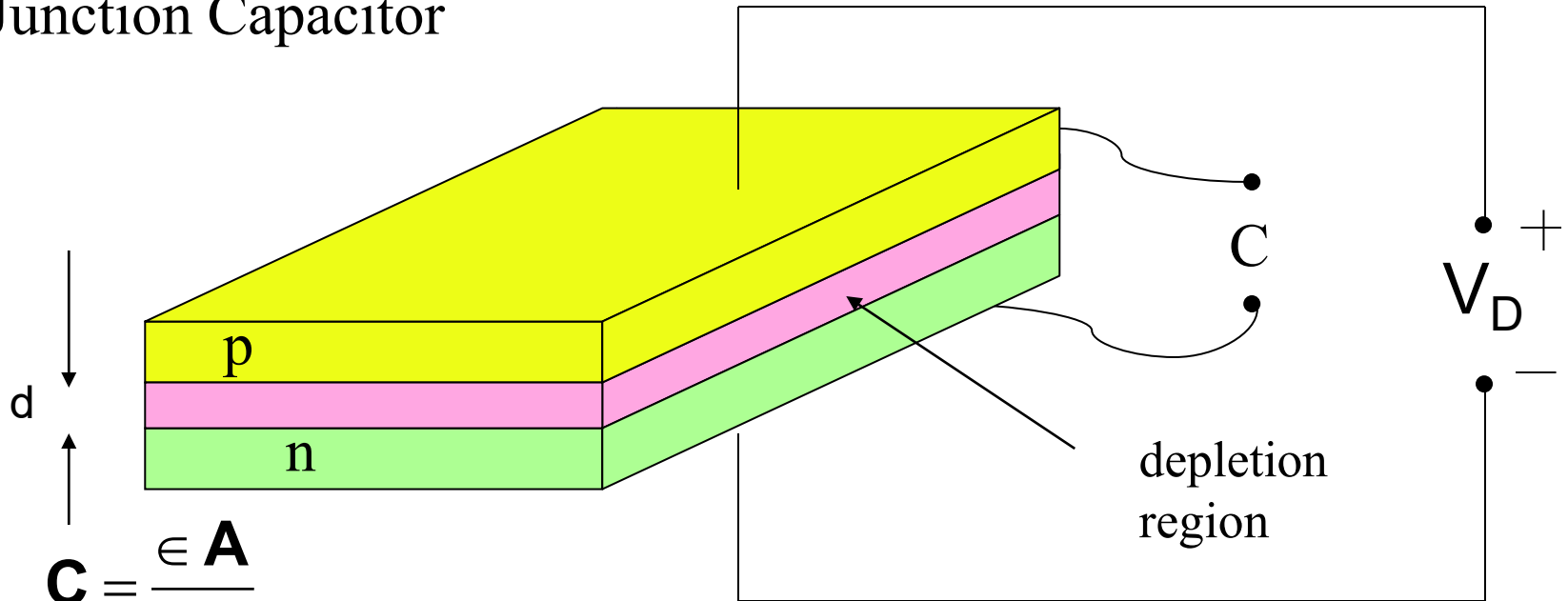
# Fringe Capacitors





# Capacitance

## Junction Capacitor



$$C = \frac{\epsilon A}{d}$$

$\epsilon$  is dielectric constant

$$C = \frac{C_{j0} A}{\left(1 - \frac{V_D}{\phi_B}\right)^n} \quad \text{for } V_{FB} < \frac{\phi_B}{2}$$

Note:  $d$  is voltage dependent

-capacitance is voltage dependent

-usually parasitic caps

-varicaps or varactor diodes exploit voltage dep. of  $C$

$C_{j0}$  is the zero-bias junction capacitance density

Model parameters  $\{C_{j0}, n, \phi_B\}$     Design parameters  $\{A\}$

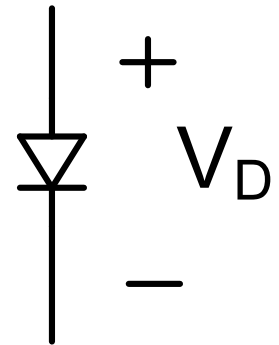
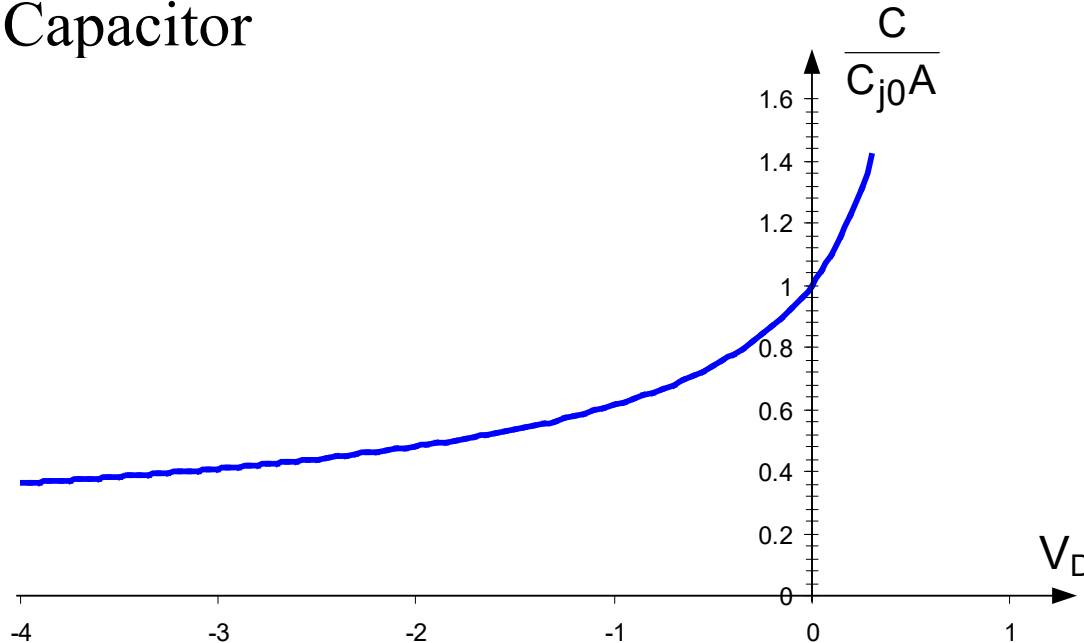
$$\phi_B \cong 0.6V$$

$$n \simeq 0.5$$

$$C_{j0} \text{ highly process dependent around } 500\text{aF}/\mu\text{m}^2$$

# Capacitance

## Junction Capacitor



$$C = \frac{C_{j0}A}{\left(1 - \frac{V_D}{\Phi_B}\right)^n} \quad \text{for } V_{FB} < \frac{\Phi_B}{2}$$

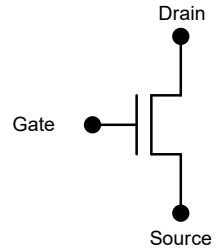
Voltage dependence is substantial

$$\Phi_B \approx 0.6V \quad n \approx 0.5$$

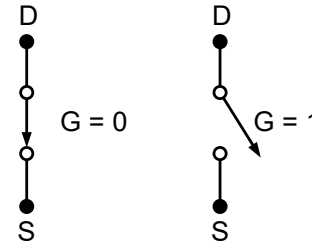
# Basic Devices and Device Models

- Resistor
- Diode
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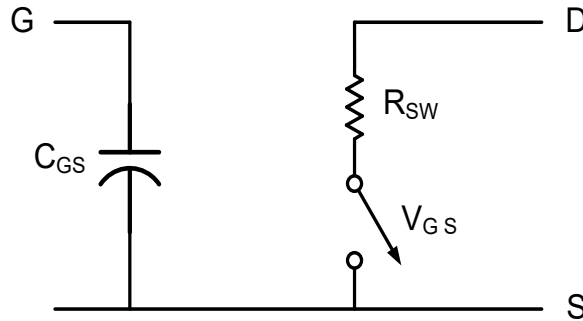
# Summary of Existing Models (for n-channel)



## 1. Switch-Level model

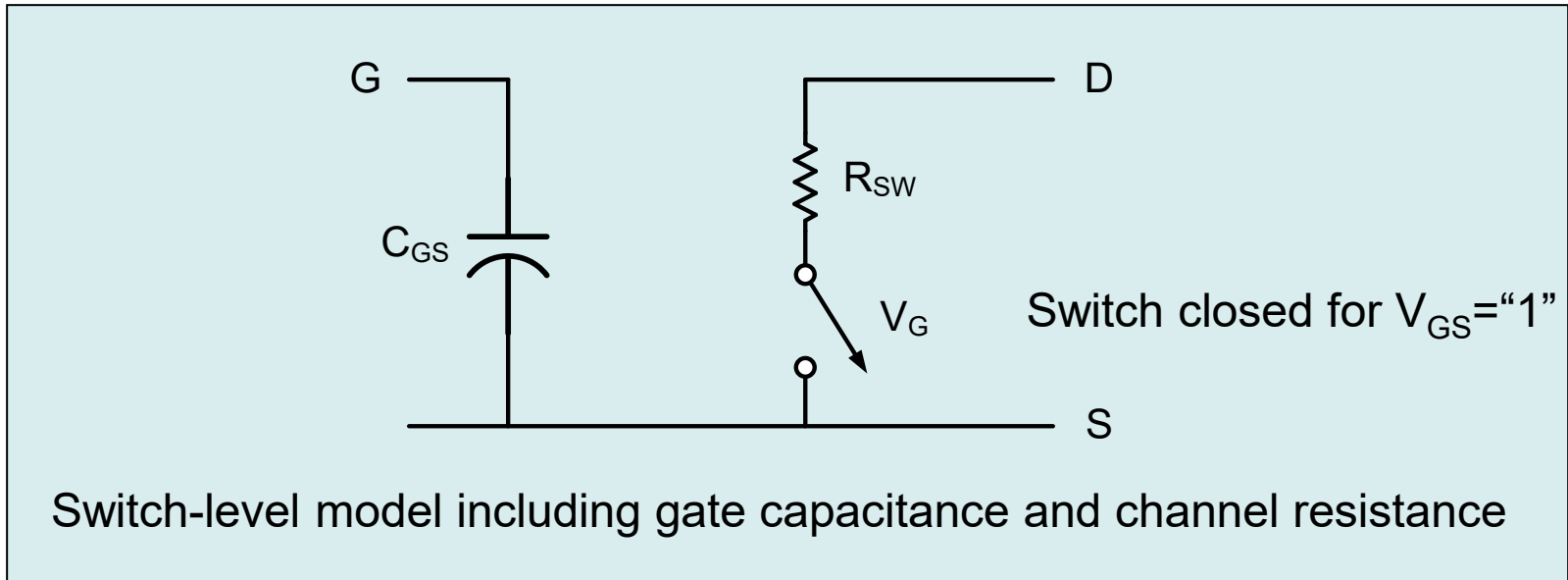


## 2. Improved switch-level model



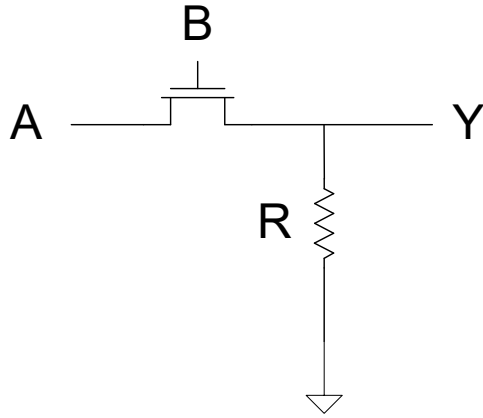
*Switch closed for  $|V_{GS}| = \text{large}$   
Switch open for  $|V_{GS}| = \text{small}$*

# Improved Switch-Level Model

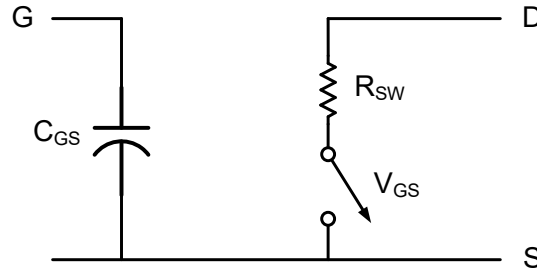


- Connect the gate capacitance to the source to create lumped model
- Still neglect bulk connection

# Limitations of Existing MOSFET Models



What is Y when A=B=VDD

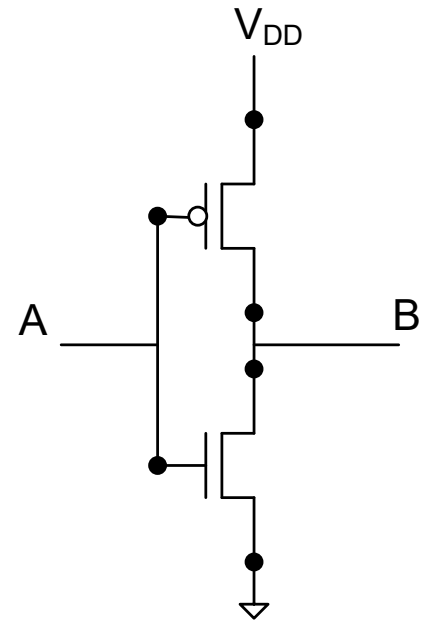


*For minimum-sized devices in a 0.5u process with  $V_{DD}=5V$*

$$C_{GS} \cong 1.5\text{fF}$$

$$R_{sw} \cong \left. \begin{array}{l} 2\text{K}\Omega \text{ n-channel} \\ 6\text{K}\Omega \text{ p-channel} \end{array} \right\}$$

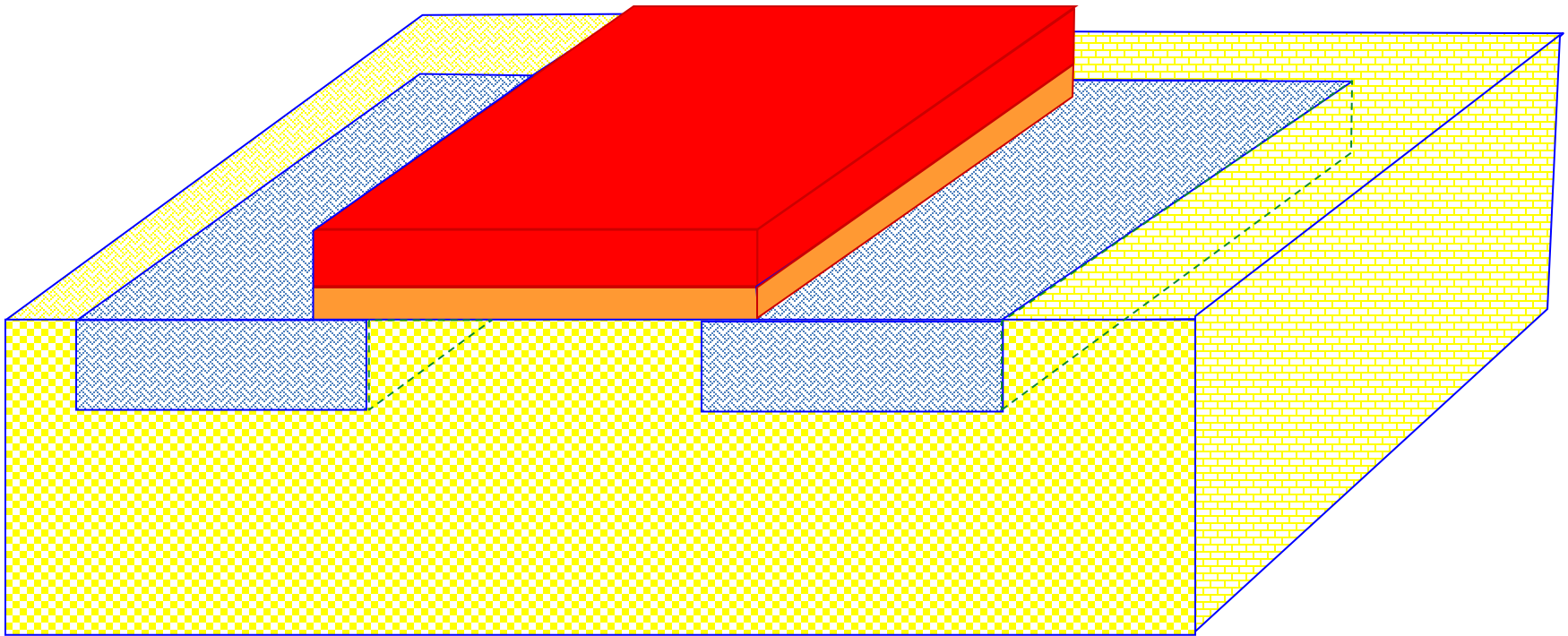
What is  $R_{sw}$  if MOSFET is not minimum sized?



What is power dissipation if A is stuck at an intermediate voltage?

**Better Model of MOSFET is Needed!**

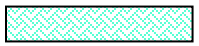
# n-Channel MOSFET



Poly



Gate oxide

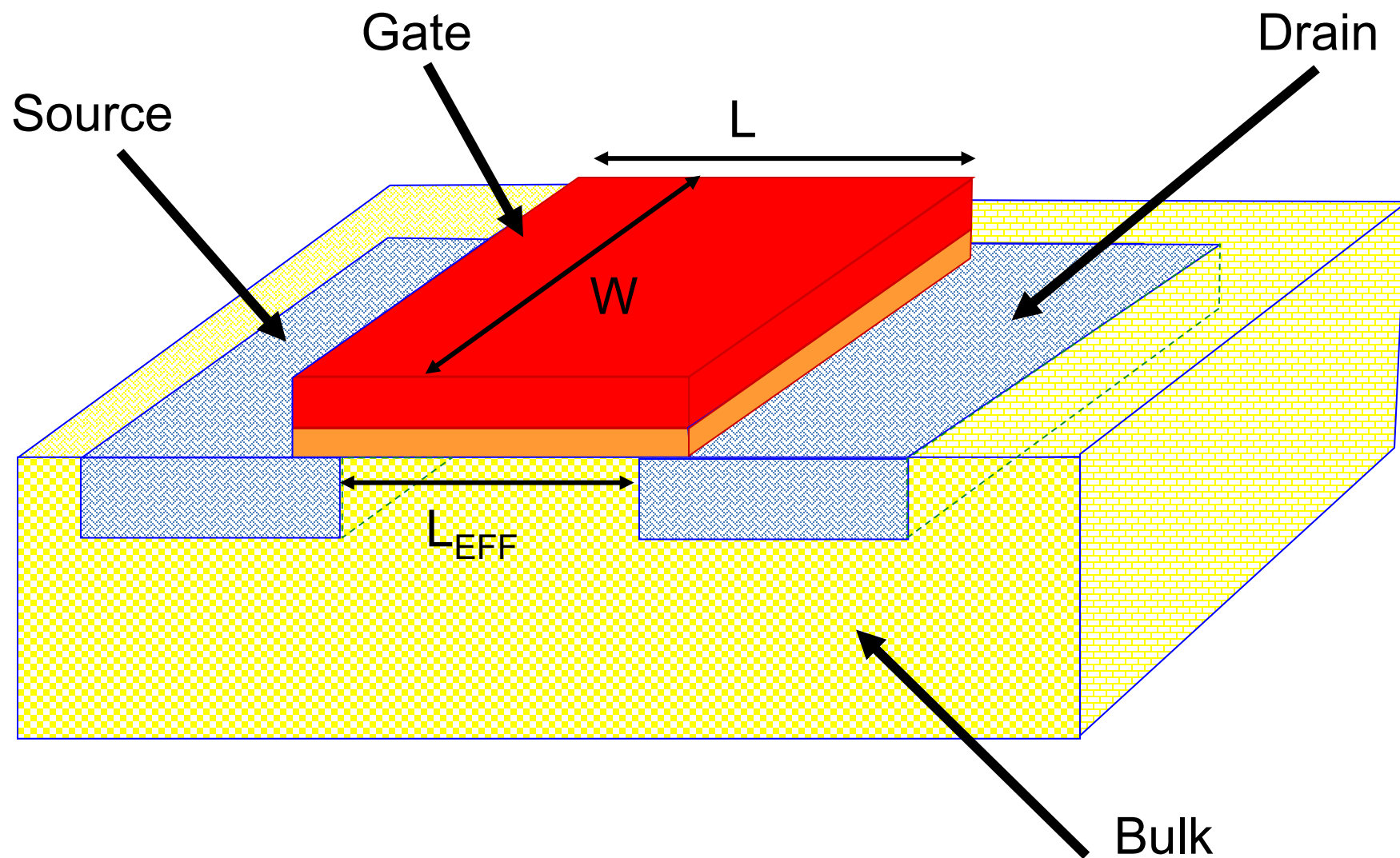


n-active



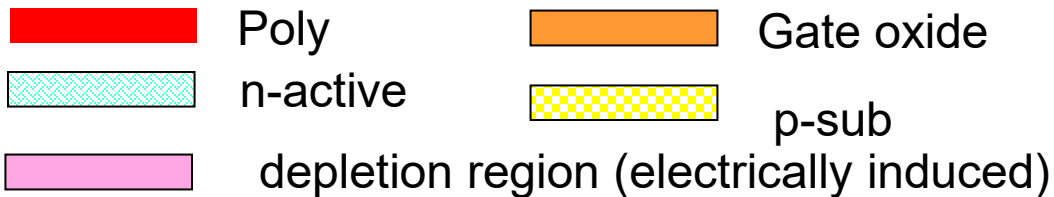
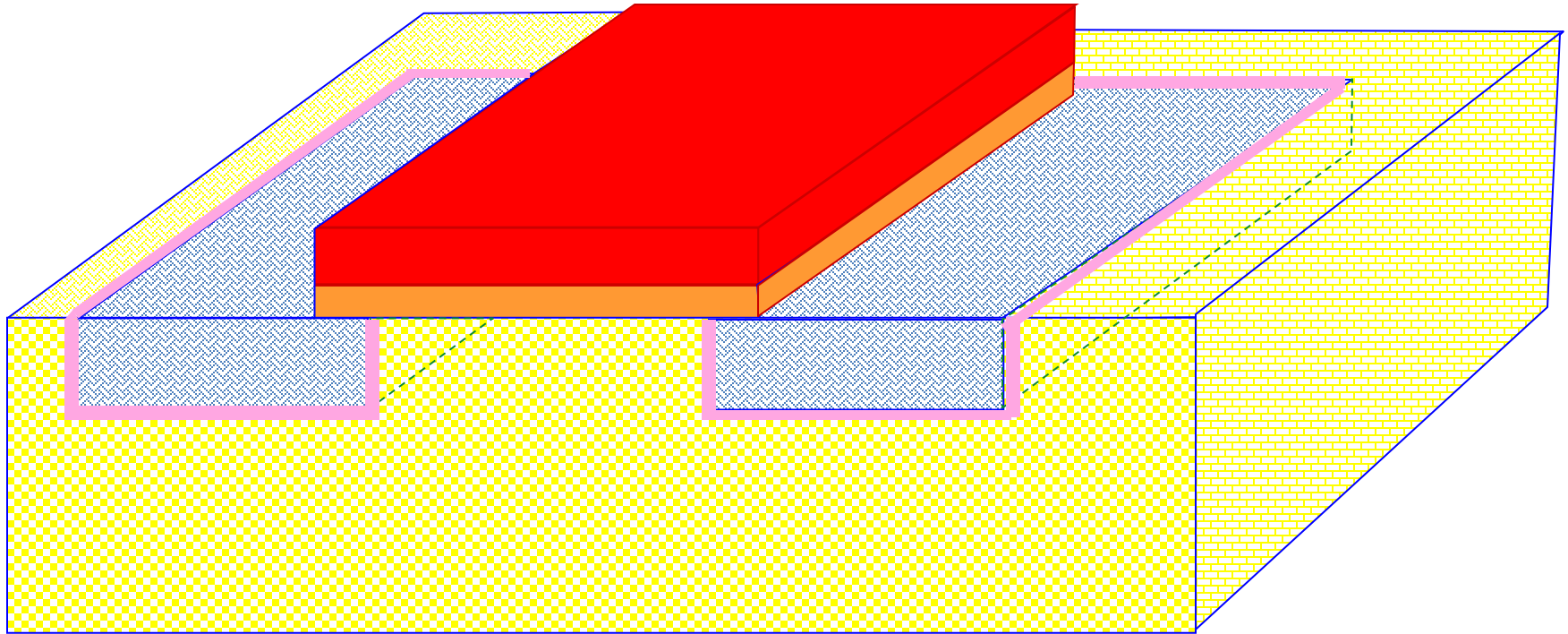
p-sub

# n-Channel MOSFET





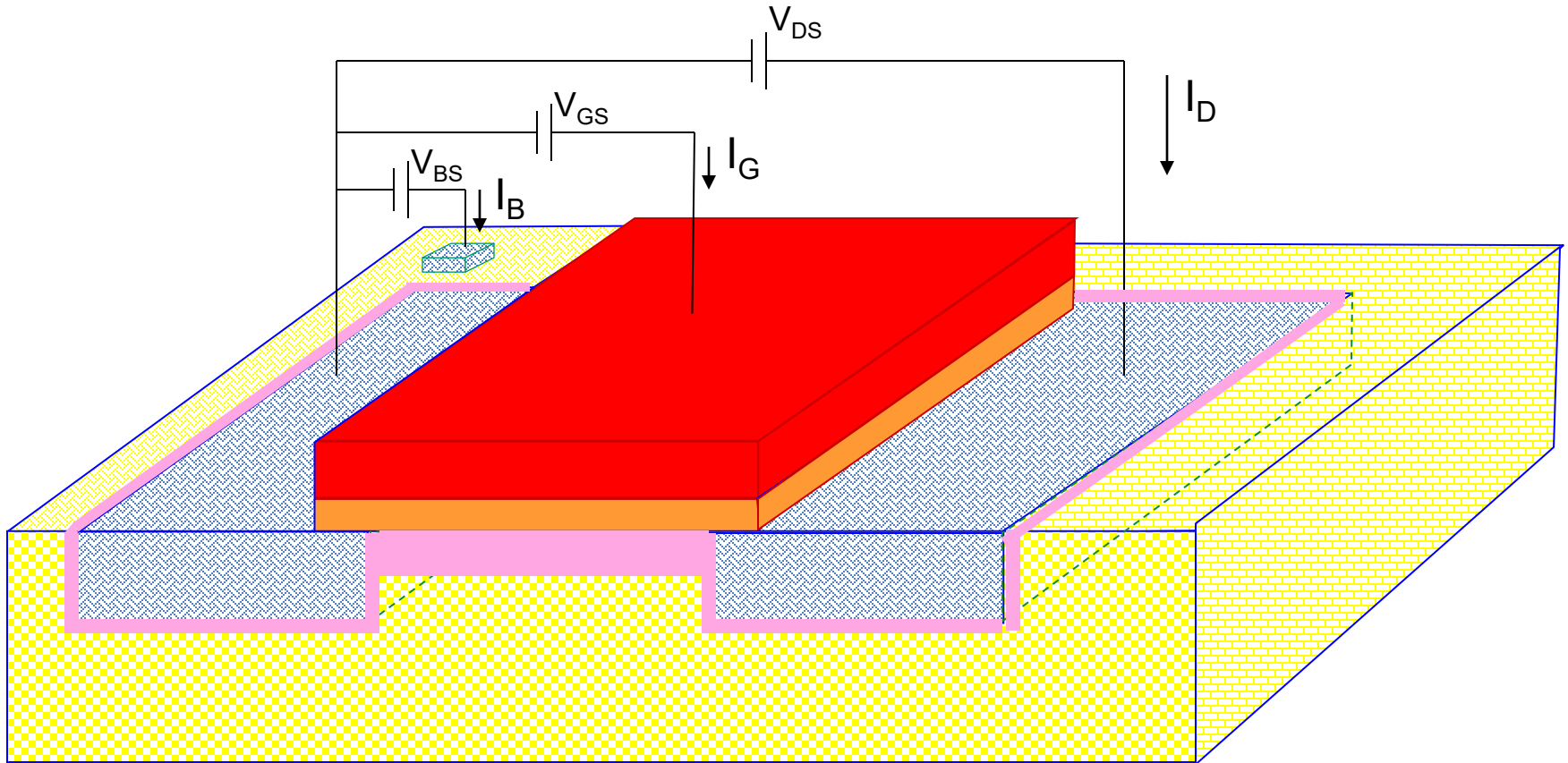
# n-Channel MOSFET



- In what follows assume all pn junctions reverse biased (almost always used this way)
- Extremely small reverse bias pn junction current can be neglected in most applications



# n-Channel MOSFET Operation and Model

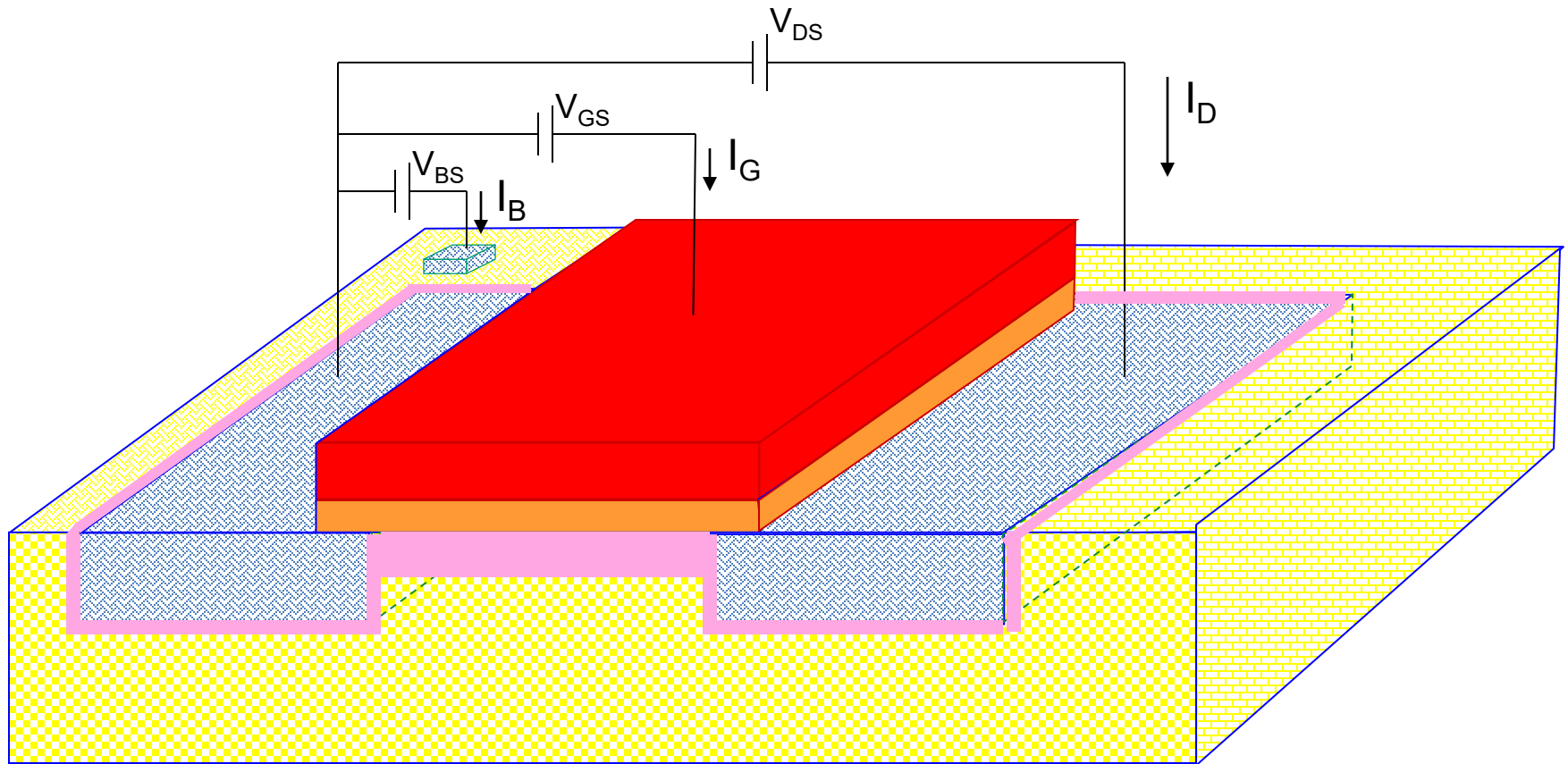


Increase  $V_{GS}$   
( $V_{DS}$  and  $V_{BS}$  assumed to be small)

Depletion region in channel becomes larger

$$\begin{aligned} I_D &= 0 \\ I_G &= 0 \\ I_B &= 0 \end{aligned}$$

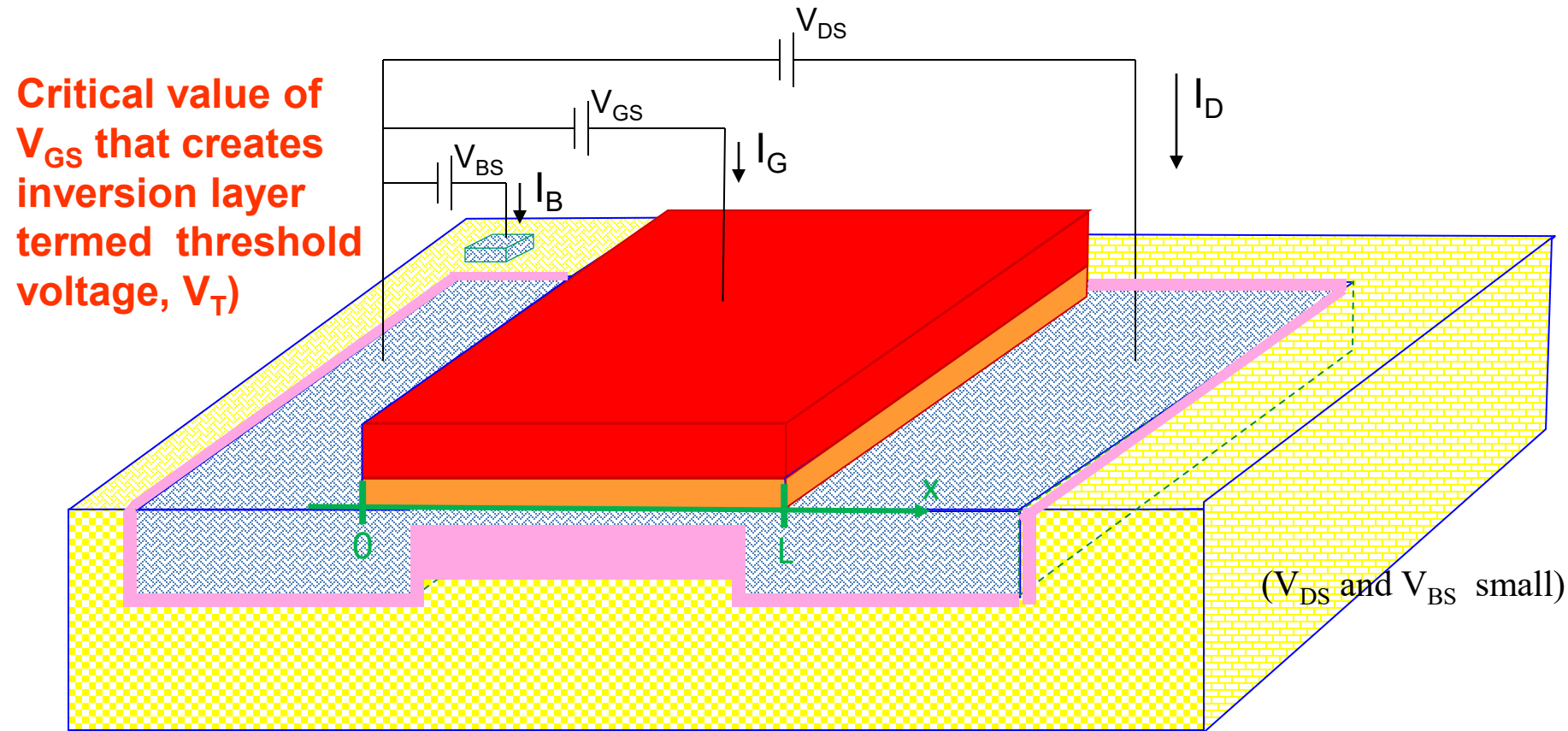
# n-Channel MOSFET Operation and Model



$$\begin{aligned} I_D &= 0 \\ I_G &= 0 \\ I_B &= 0 \end{aligned}$$

Model in Cutoff Region

# n-Channel MOSFET Operation and Model



Increase  $V_{GS}$  more

Inversion layer forms in channel

Inversion layer will support current flow from D to S

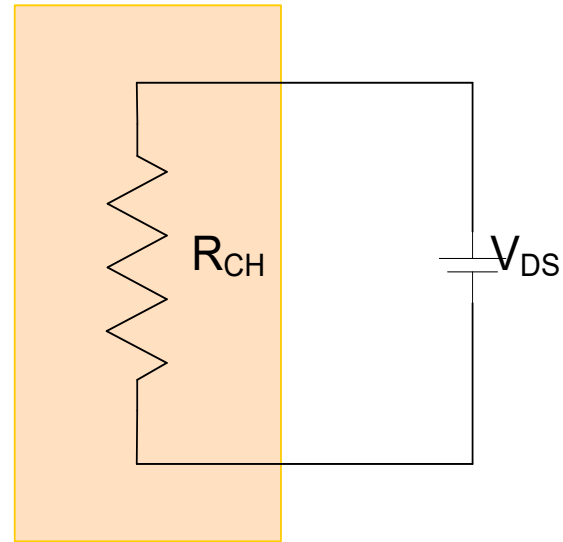
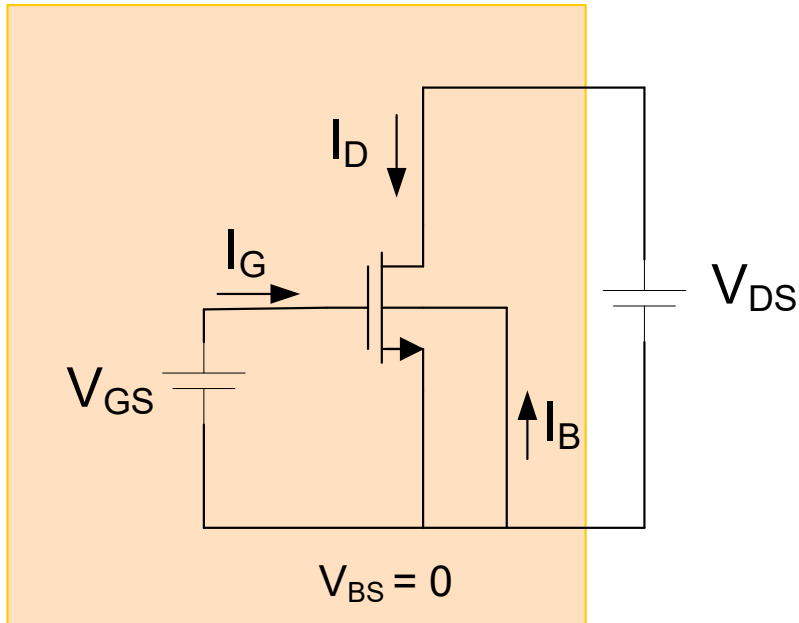
Channel behaves as thin-film resistor

$$I_D R_{CH} = V_{DS}$$

$$I_G = 0$$

$$I_B = 0$$

# Triode Region of Operation



For  $V_{DS}$  small

$$R_{CH} = \frac{L}{W} \frac{1}{(V_{GS} - V_{TH}) \mu C_{OX}}$$

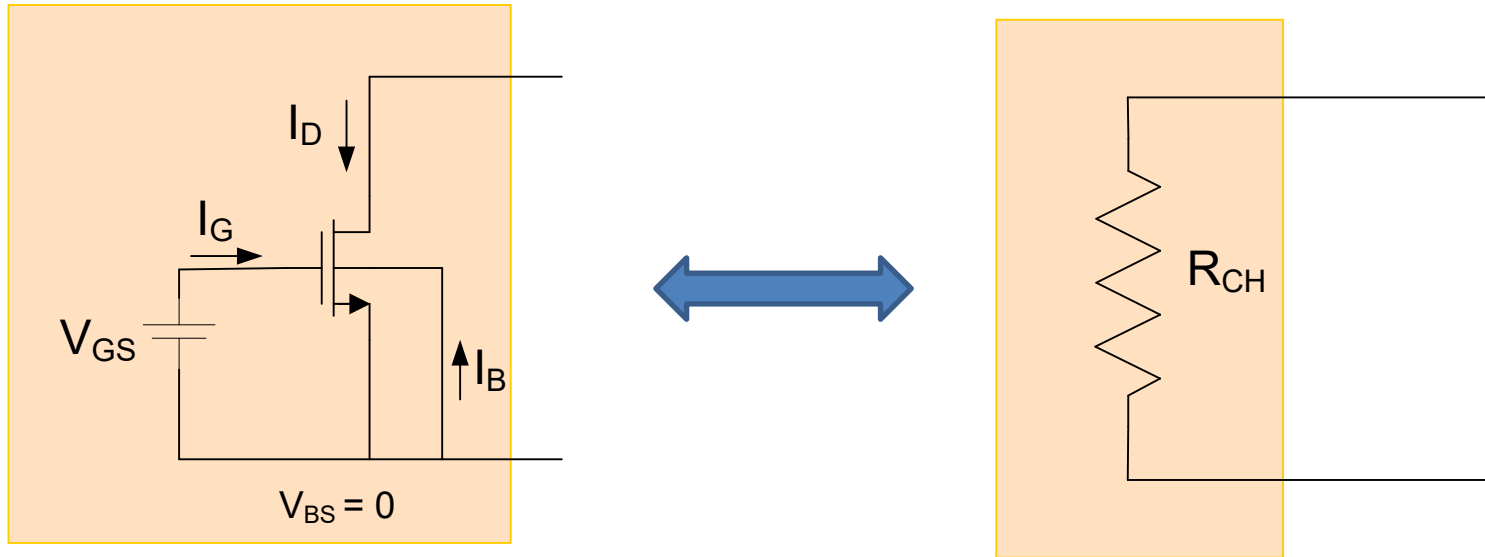
Behaves as a resistor between drain and source

$$I_D = \mu C_{OX} \frac{W}{L} (V_{GS} - V_{TH}) V_{DS}$$

$$I_G = I_B = 0$$

Model in Deep Triode Region

# Triode Region of Operation

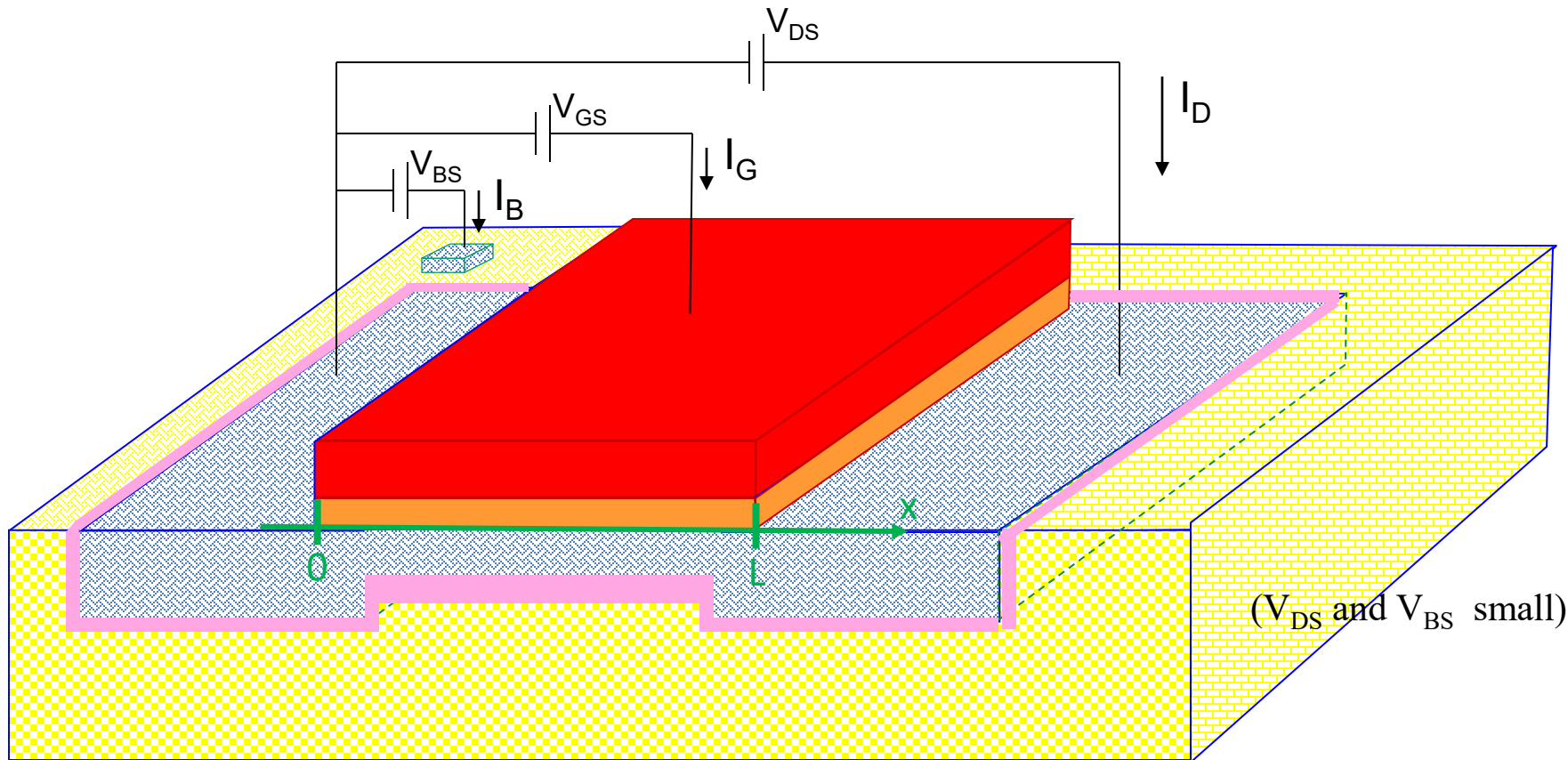


For  $V_{DS}$  small

$$R_{CH} = \frac{L}{W} \frac{1}{(V_{GS} - V_{TH}) \mu C_{OX}}$$

Resistor is controlled by the voltage  $V_{GS}$   
Termed a “Voltage Controlled Resistor” (VCR)

# n-Channel MOSFET Operation and Model



$V_{GC}(x)$  approx. constant for small  $V_{DS}$

Increase  $V_{GS}$  more

Inversion layer in channel thickens

$R_{CH}$  will decrease

Termed “ohmic” or “triode” region of operation

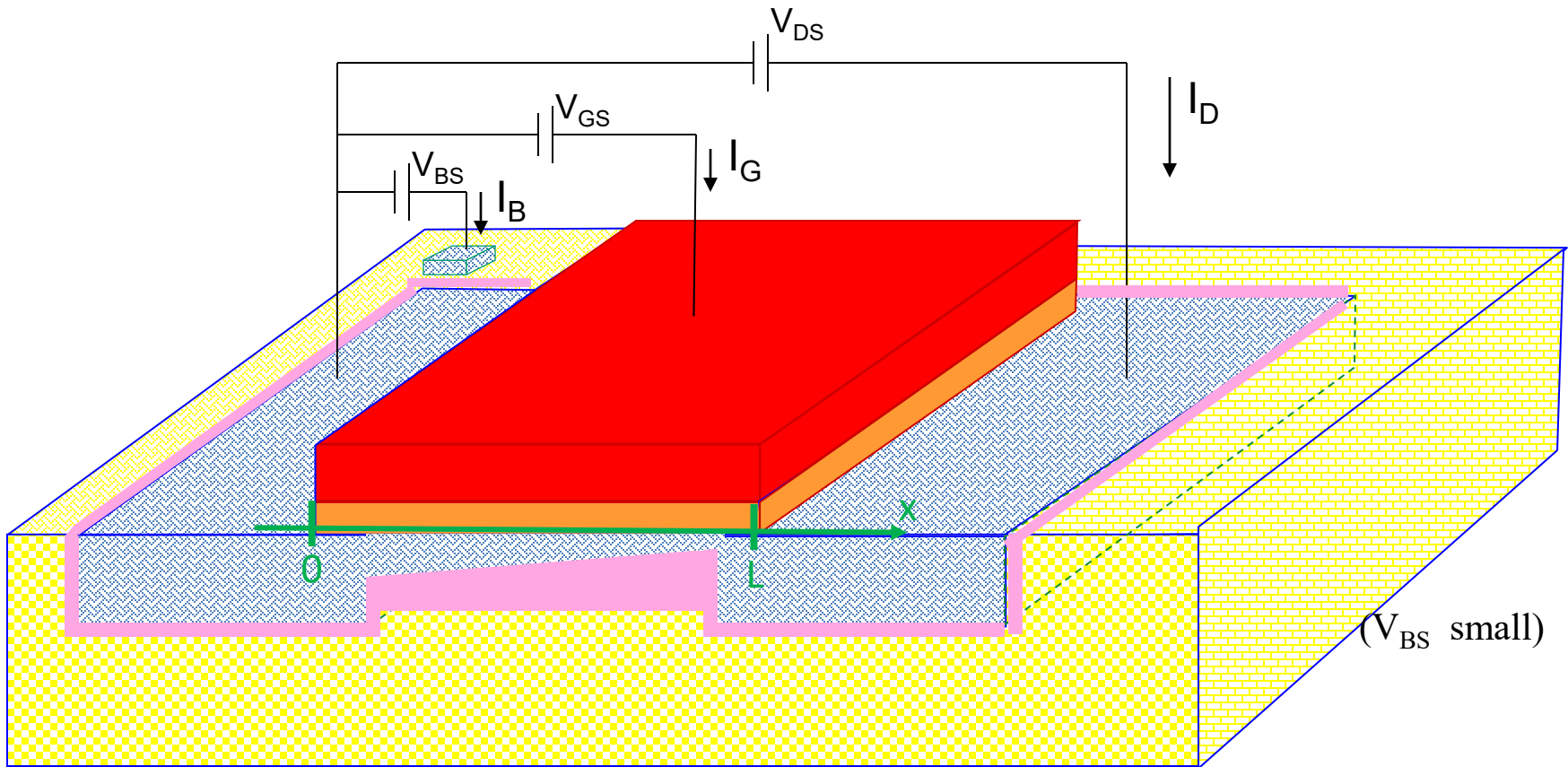
$$I_D R_{CH} = V_{DS}$$

$$I_G = 0$$

$$I_B = 0$$



# n-Channel MOSFET Operation and Model



Increase  $V_{DS}$

$V_{GC}(x)$  changes with  $x$  for larger  $V_{DS}$

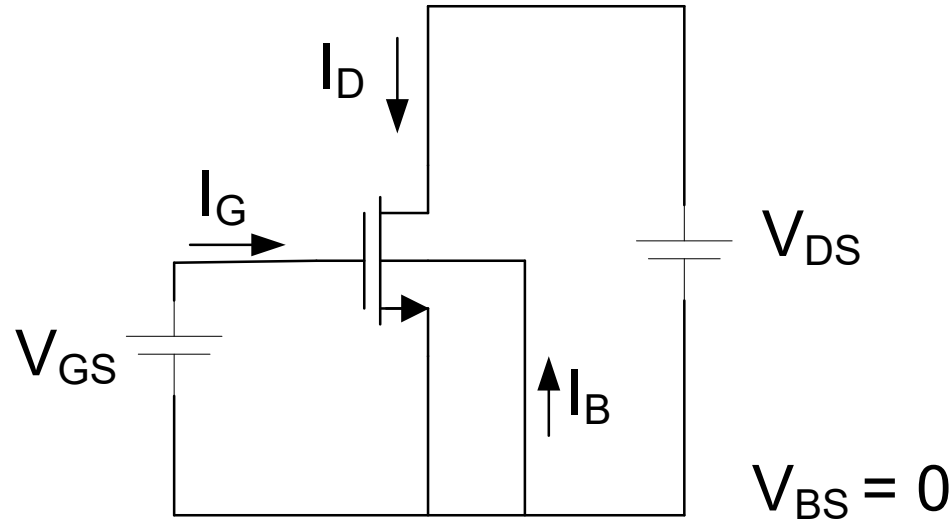
Inversion layer thins near drain  
 $I_D$  no longer linearly dependent upon  $V_{DS}$   
 Still termed “ohmic” or “triode” region of operation

$$I_D = ?$$

$$I_G = 0$$

$$I_B = 0$$

# Triode Region of Operation



For  $V_{DS}$  larger

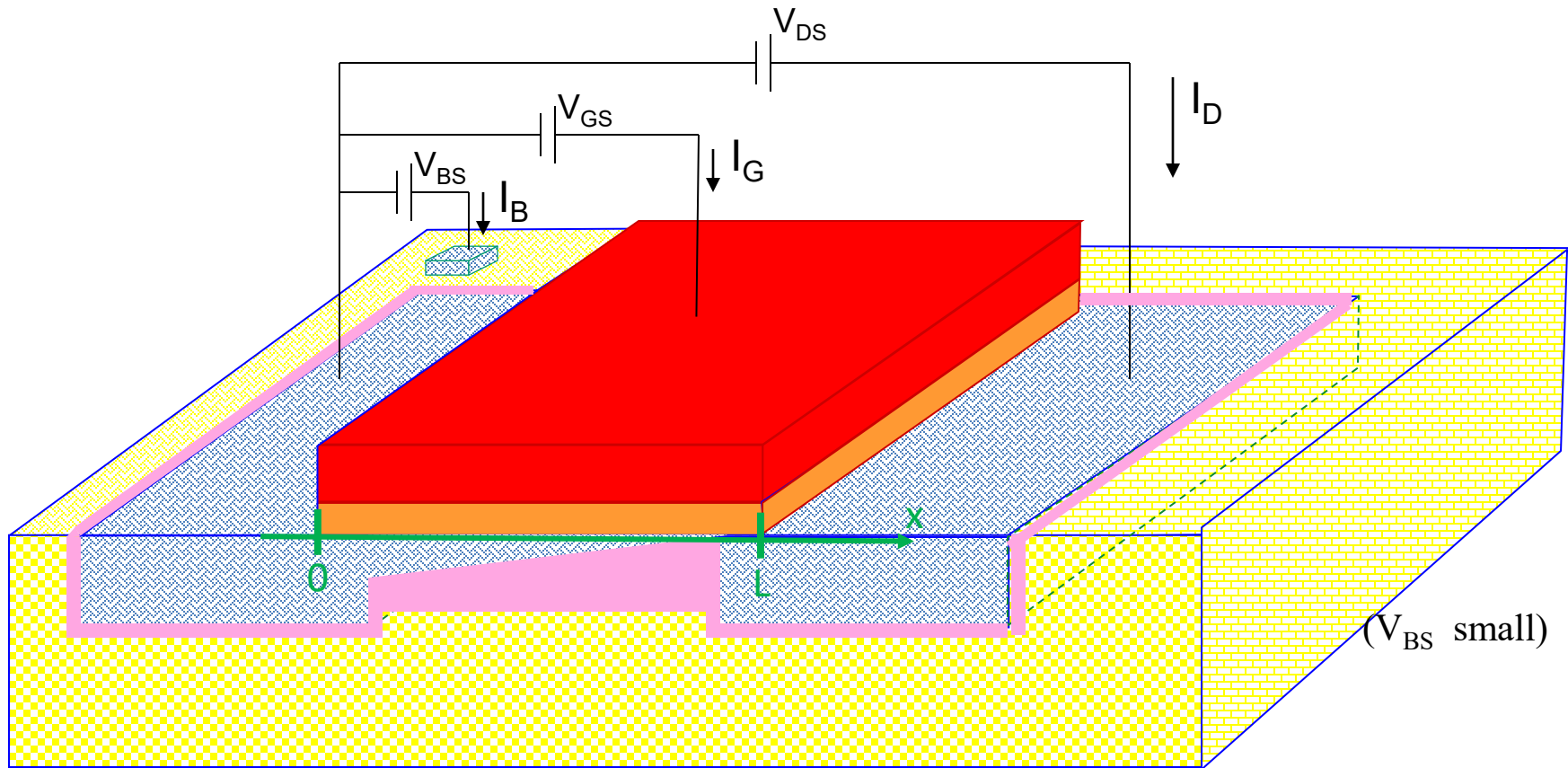
~~$$R_{CH} = \frac{L}{W (V_{GS} - V_{TH}) \mu C_{OX}}$$~~

$$I_D = \mu C_{OX} \frac{W}{L} \left( V_{GS} - V_{TH} - \frac{V_{DS}}{2} \right) V_{DS}$$

$$I_G = I_B = 0$$

Model in Triode Region

# n-Channel MOSFET Operation and Model



Increase  $V_{DS}$  even more

$V_{GC}(L) = V_{TH}$  when channel saturates

Inversion layer disappears near drain

Termed "saturation" region of operation

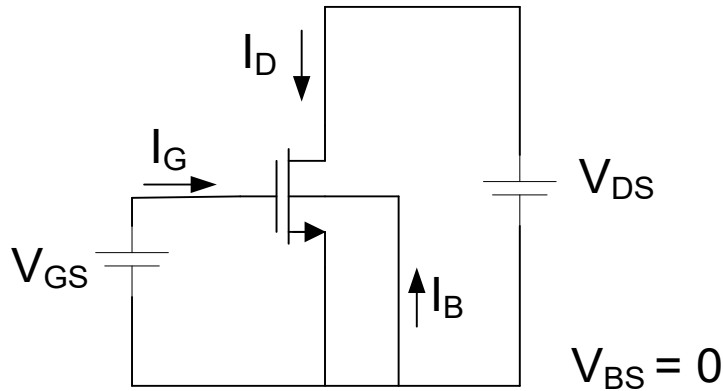
Saturation first occurs when  $V_{DS} = V_{GS} - V_{TH}$

$$I_D = ?$$

$$I_G = 0$$

$$I_B = 0$$

# Saturation Region of Operation



$$I_D = \mu C_{OX} \frac{W}{L} \left( V_{GS} - V_{TH} - \frac{V_{DS}}{2} \right) V_{DS}$$

*or equivalently*

$$I_D = \mu C_{OX} \frac{W}{L} \left( V_{GS} - V_{TH} - \frac{V_{GS} - V_{TH}}{2} \right) (V_{GS} - V_{TH})$$

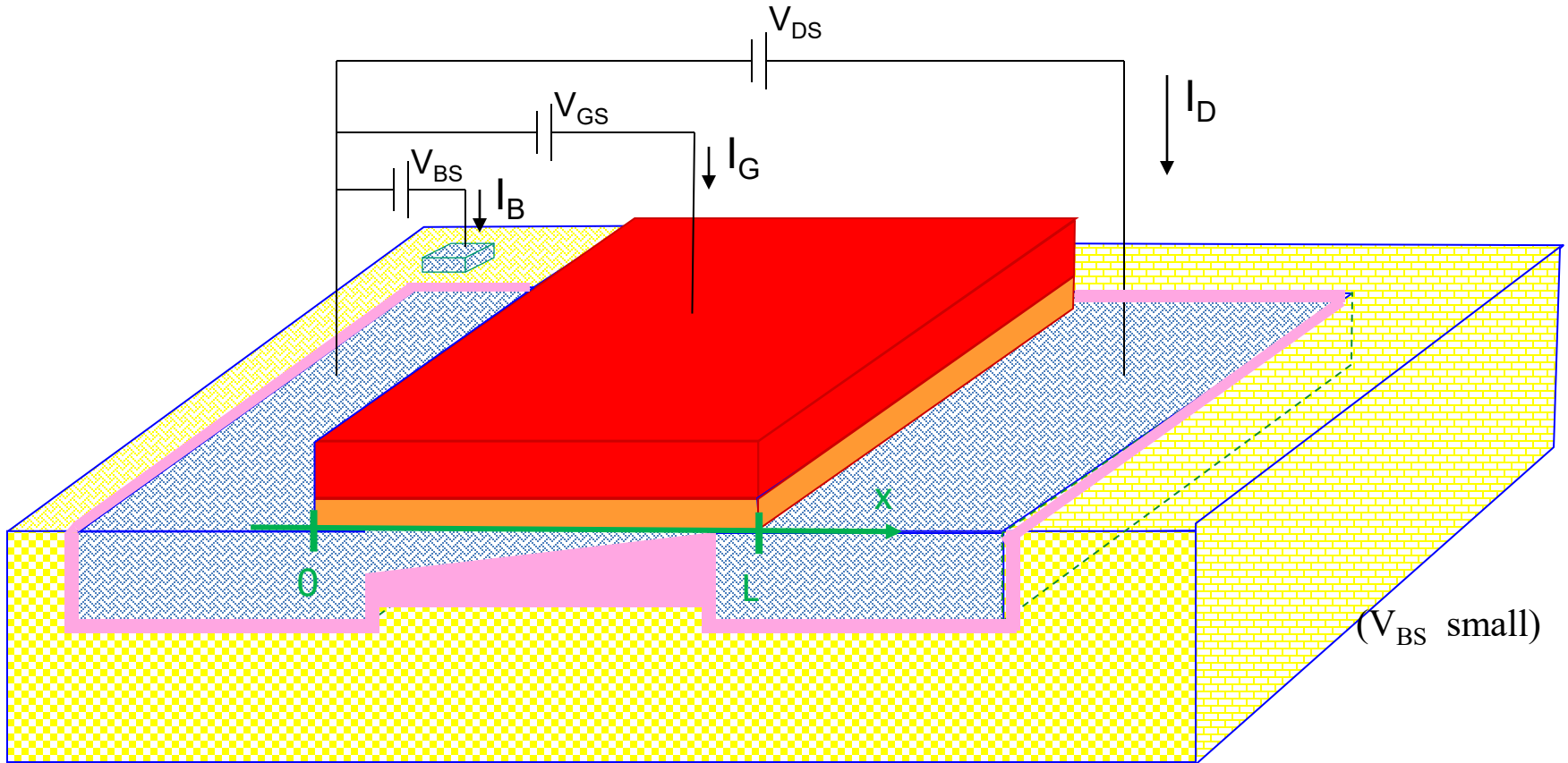
*or equivalently*

$$I_D = \frac{\mu C_{OX} W}{2L} (V_{GS} - V_{TH})^2$$

$$I_G = I_B = 0$$

For  $V_{DS}$  at onset of saturation

# n-Channel MOSFET Operation and Model



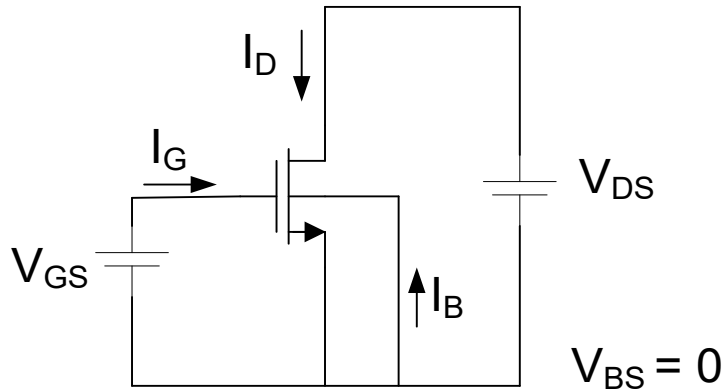
Increase  $V_{DS}$  even more (beyond  $V_{GS} - V_{TH}$ )

Nothing much changes !!

Termed “saturation” region of operation

$$\begin{aligned} I_D &=? \\ I_G &=0 \\ I_B &=0 \end{aligned}$$

# Saturation Region of Operation



For  $V_{DS}$  in Saturation

$$I_D = \frac{\mu C_{OX} W}{2L} (V_{GS} - V_{TH})^2$$

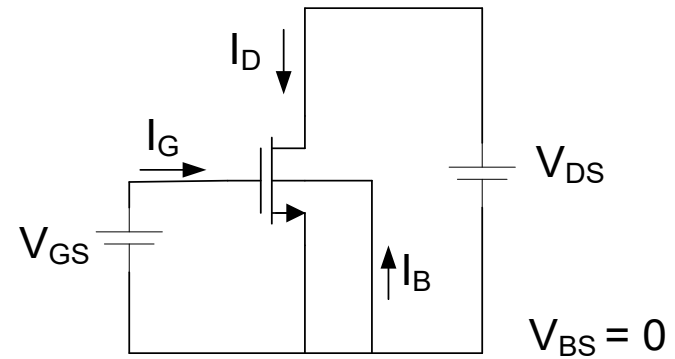
$$I_G = I_B = 0$$

Model in Saturation Region

# Model Summary

n-channel MOSFET

Notation change:  $V_T = V_{TH}$ , don't confuse  $V_T$  with  $V_t = kT/q$



$$I_D = \begin{cases} 0 & V_{GS} \leq V_{TH} & \text{Cutoff} \\ \mu C_{OX} \frac{W}{L} \left( V_{GS} - V_{TH} - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \geq V_{TH} \quad V_{DS} < V_{GS} - V_{TH} & \text{Triode} \\ \mu C_{OX} \frac{W}{2L} (V_{GS} - V_{TH})^2 & V_{GS} \geq V_{TH} \quad V_{DS} \geq V_{GS} - V_{TH} & \text{Saturation} \end{cases}$$

$$I_G = I_B = 0$$

Model Parameters:  $\{\mu, V_{TH}, C_{OX}\}$  Design Parameters :  $\{W, L\}$

This is a piecewise model (not piecewise linear though)

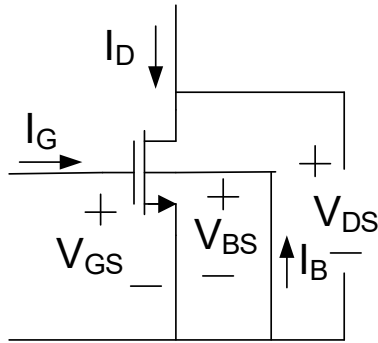
Piecewise model is continuous at transition between regions

(Deep triode special case of triode where  $V_{DS}$  is small  $R_{CH} = \frac{L}{W} \frac{1}{(V_{GS} - V_{TH}) \mu C_{OX}}$ )

**Note: This is the third model we have introduced for the MOSFET**

# Model Summary

n-channel MOSFET



$V_{BS} = 0$

$$I_D = \begin{cases} 0 & V_{GS} \leq V_{TH} \\ \mu C_{OX} \frac{W}{L} \left( V_{GS} - V_{TH} - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \geq V_{TH} \quad V_{DS} < V_{GS} - V_{TH} \\ \mu C_{OX} \frac{W}{2L} (V_{GS} - V_{TH})^2 & V_{GS} \geq V_{TH} \quad V_{DS} \geq V_{GS} - V_{TH} \end{cases}$$

$$V_{GS} \leq V_{TH}$$

$$V_{GS} \geq V_{TH} \quad V_{DS} < V_{GS} - V_{TH}$$

$$V_{GS} \geq V_{TH} \quad V_{DS} \geq V_{GS} - V_{TH}$$

$$I_G = I_B = 0$$

Observations about this model (developed for  $V_{BS}=0$ ):

$$I_D = f_1(V_{GS}, V_{DS})$$

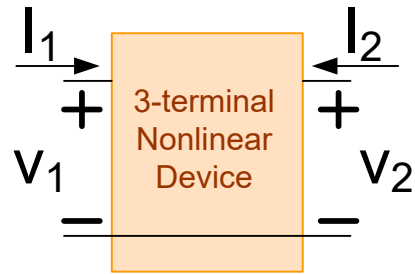
$$I_G = f_2(V_{GS}, V_{DS})$$

$$I_B = f_3(V_{GS}, V_{DS})$$

This is a nonlinear model characterized by the functions  $f_1$ ,  $f_2$ , and  $f_3$  where we have assumed that the port voltages  $V_{GS}$  and  $V_{DS}$  are the independent variables and the drain currents are the dependent variables



# General Nonlinear Models

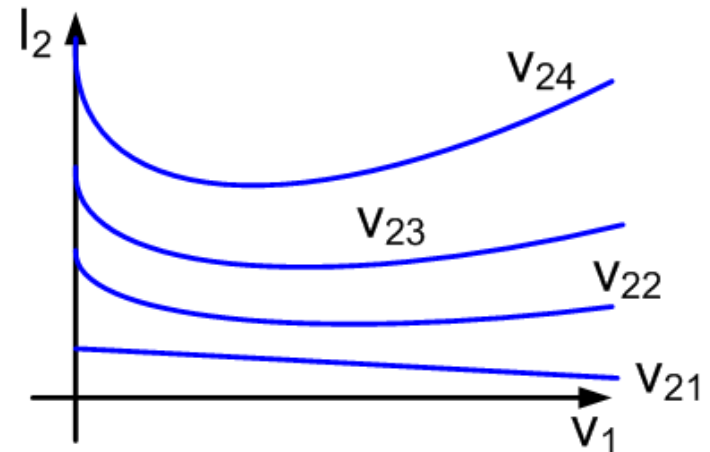
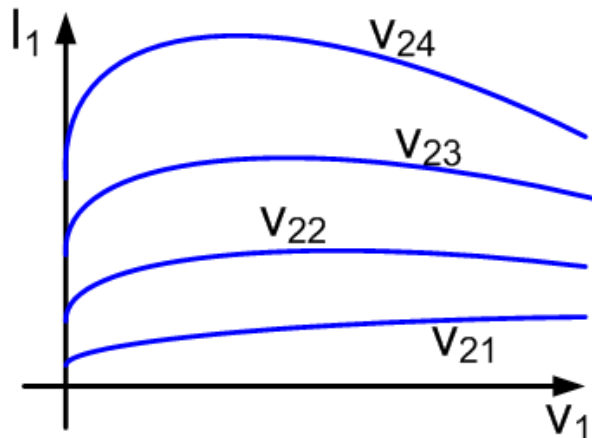


$$I_1 = f_1(V_1, V_2)$$

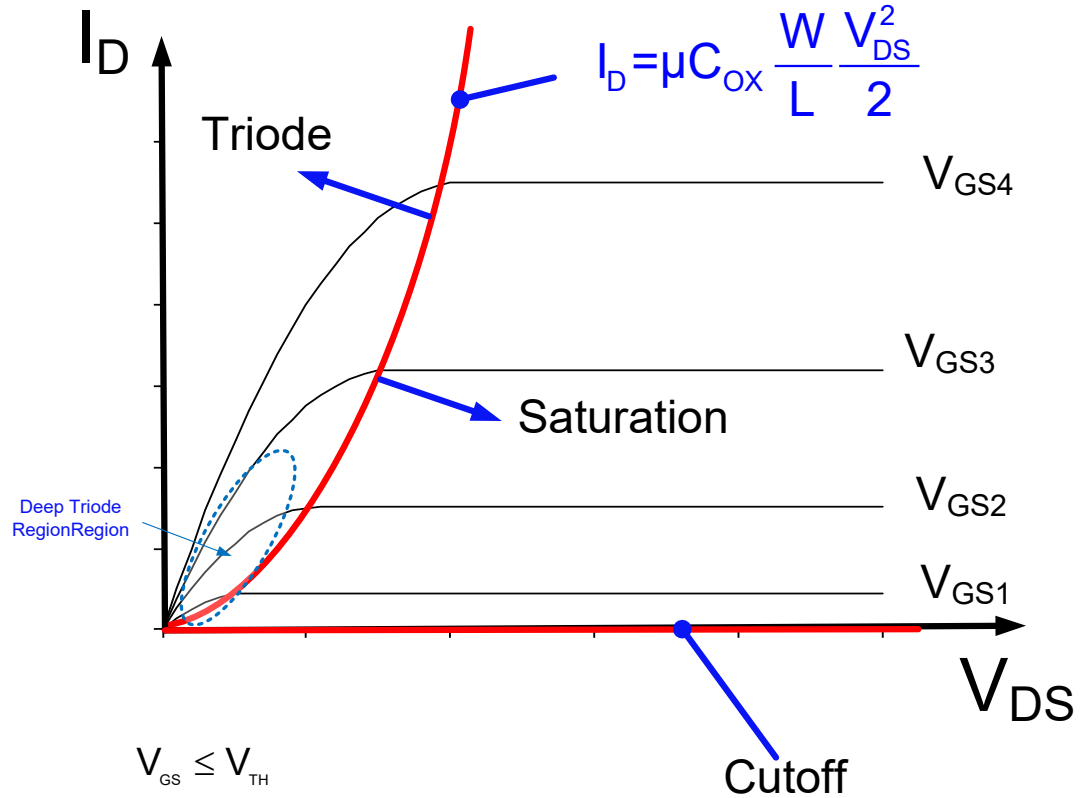
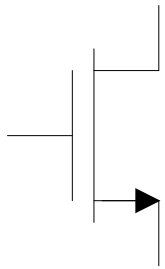
$$I_2 = f_2(V_1, V_2)$$

$I_1$  and  $I_2$  are 3-dimensional relationships which are often difficult to visualize

Two-dimensional representation of 3-dimensional relationships



# Graphical Representation of MOS Model



$$I_D = \begin{cases} 0 & V_{GS} \leq V_{TH} \\ \mu C_{ox} \frac{W}{L} \left( V_{GS} - V_{TH} - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \geq V_{TH} \quad V_{DS} < V_{GS} - V_{TH} \\ \mu C_{ox} \frac{W}{2L} (V_{GS} - V_{TH})^2 & V_{GS} \geq V_{TH} \quad V_{DS} \geq V_{GS} - V_{TH} \end{cases}$$

$$I_G = I_B = 0$$

Parabola separated triode and saturation regions and corresponds to  $V_{DS} = V_{GS} - V_{TH}$



Stay Safe and Stay Healthy !

End of Lecture 16